EXHIBIT A

DRAFT OF AMERICAN NATIONAL STANDARD FOR TELECOMMUNICATIONS DIGITAL HIERARCHY OPTICAL INTERFACE RATES AND FORMATS SPECIFICATIONS

Secretariat:

EXCHANGE CARRIERS STANDARDS ASSOCIATION
T1 COMMITTEE-TELECOMMUNICATIONS

Approved: [date to be inserted]

Abstract:

The purpose of this standard is to establish specifications for a rate and format of a signal which will be used in optical interfaces. Moreover, this standard will define a base rate and format with a multiplexing scheme such that an entire family of rates and formats for optical interfaces will be established. This standard will specifically establish the rate and format in what could be considered an electrical domain; however, it is not intended that this standard serve as an electrical interface specification. A companion standard, American National Standard For Telecommunications Digital Hierarchy Optical Interface Specifications: Single-Mode, establishes the optical parameters to be used in conjunction with this rate and format to define an optical interface.

Foreword:

(This foreword is not a part of American National Standard for Telecommunications Digital Hierarchy Optical Interface Rates and Formats Specifications)

This standard was initiated by the Interexchange Carrier Compatibility Forum (ICCF) in May, 1984 as a long term solution to an optical mid-span meet between interexchange and exchange carriers. As much flexibility as possible has been built into the specification to allow technical innovation but still provide compatibility.

Suggestions for improvement of this standard will be welcome. They should be sent to the Exchange Carriers Standards Association, Suite 200, 5430 Grosvenor Lane, Bethesda, MD 20814-2122.

This standard was processed and approved for submittal to ANSI by Accredited Standards Committee T1 - Telecommunications. Committee approval of the standard does not necessarily imply that all committee members voted for its approval. At the time it approved this standard, Accredited Standards Committee T1 had the following members:

(List of T1 Committee officers and Organizations Represented including names of Voting and Alternate Representatives to be provided by ECSA after T1 letter ballot)

At the time it approved this standard, the Technical Subcommittee T1X1 on Carrier to Carrier Interfaces had the following members:

Jim Bradley, Chair
David W. Jurling, Vice-Chair
Erik Hansson, Secretary

ORGANIZATION REPRESENTED	NAME OF REPRESENTATIVE
ADC Telecommunications Inc.	Richard Masloski
	Dennis Burroughs (Alt)
Alcatel Network Systems Corp	Harold Goodnight
	Lynn Bishop (Alt)
Amdahl Communications	Farooq Raza
	Dieter Nattkemper (Alt)
Ameritech Services Inc.	Larry A. Young
	Erick W. Rozier (Alt)
AMP Incorporated	George Lawrence
	Bernie Caron (Alt)
AT&T Communications	Gerald H. Peterson
	P.L. Bryan (Alt)
AT&T Technologies	W.F. Robinson
	S.J. Chen (Alt)
Austron Incorporated	Robert F. Ellis
BDM Corporation	Roy Bernd

ORGANIZATION REPRESENTED	NAME OF REPRESENTATIVE
Bell Atlantic	Joseph J. Lischka (Alt)
	Martin Carroll
	Frank Klopfer (Alt)
Bellcore	J.C. Staats
	G.G. Schlanger (Alt)
BellSouth Services	Rick C. McNealy
	John W. Fox (Alt)
CNCP Telecommunications	Libor F. Susil
	Elias Lafazanos (Alt)
Communications Transmission Inc	Walter G. Lammert
	Stephen D. Klingler (Alt)
Computer Consoles Inc	Kenneth P. Sympson
	S. Ron Foster (Alt)
COMSAT Corporation	Ben Levitan
	Stephen J. Engelman (Alt)
Contel Corporation	Steve Linskey
	Russell G. DeWitt (Alt)
Creative Communications Consulting	Richard Bobilin
	James Boe (Alt)
Defense Communications Agency	George Moran
	Michael DeFrancesco (Alt)
Digitech Communications Inc	Roger F. Atkinson
	Robert A. Brown (Alt)
DSC Communications Corp	Gene Larman
	Sid Ghosh (Alt)
Ericsson Incorporated	Par Bragwad
	Roselyne Genin (Alt)
Fujitsu America Inc	Roger Pandanda
	S. Minneman (Alt)
GTE Communication Systems Corp	Brian Foster
	J.D. Peterson (Alt)
GTE SC/Telephone Operations	Conferlete Carney
	D.J. Kostas (Alt)
Hekimian Laboratories	Larry E. Keith
	Jonathan C. Kim (Alt)
IBM Corporation	Rata P. Piplani
	Robert M. Amy (Alt)
Integrated Technology Inc	Mark Lanning
	Dave Hensley (Alt)
LICOM Incorporated	Lynn Chapman
M/A-COM Corporation	Michael Sun
Martin Marietta Info. & Commun	W. Fred Seigneau
	J. Horrell (Alt)
MCI Telecommunications Corp	Yi-Shang Shen
	Gustaf Ehrner (Alt)
Motorola Inc	Ken Felix
	Jim Williams (Alt)

ORGANIZATION REPRESENTED	NAME OF REPRESENTATIVE
National Communications Systems	Edward Greene
	Robert M. Fenichel (Alt)
NEC America Inc	Ivan Tunon
	I. Matsuda (Alt)
Northern Telecom Incorporated	David R. Cairns
	Bruce Stevenson (Alt)
NYNEX Service Company	J.P. Burkitt
	Bruce Johnson (Alt)
Pacific Bell	Eileen M. Healy
Rockwell International Corp	Charles E. Huffman
	Everett Turvey (Alt)
Siemens Communication Sys. Inc	Ben Wagner
	Ken Prescher (Alt)
Southern New England Telephone	D.M. Murphy
Southwestern Bell Telephone Co	Barbara Engel Smith
	Ray Bretthauer (Alt)
Stromberg-Carlson Corporation	D. Edinger
Telco Systems Incorporated	Mawlin Yeh
	Thomas R. Heimes (Alt)
Telecom Canada	Joseph Chang
	Kenneth Moisey (Alt)
Telinq Systems Incorporated	Jeff Foust
	Robert Felice (Alt)
Timeplex Incorporated	Shue-Yu Kwan
	C. Tsai (Alt)
United Telephone System Inc	Lucian V. Deas
	Harold Fuller (Alt)
US Sprint	David W. Jurling
	Peter J. May (Alt)
US West	James L. Eitel
	James Dahl (Alt)
Verilink Corporation	William J. Buckley
Wang Laboratories Inc	Ming Lee
	Steve Dye (Alt)
Western Union Telegraph Co	Jacob Rabinowitz

Working Group T1X1.4, which developed this standard, had the following members:

Charles E. Huffman	Chairman
Everett J.Turvey	Vice-Chairman
Phillip Johnson	Secretary
Kevin Pickles	Co-Convener, Optical Rates and Formats Subworking Group
Yau Ching	Co-Convener, Optical Rates and Formats Subworking Group

NAME OF REPRESENTATIVE

Dr. Ghani Abbas
Hassan Ahmed
Dr. Jamil M. Ahmed
Brent Allen
Howard Altman
Richard H. Anderson
Eric H. Angell
Koichi Asatani
John Bailey
Ralph Ballart
Bert E. Basch
Gordon W. Beall
Robert L. Beebe
K. Ray Belford
Malcolm Betts
Ajaib Bhadare
Chris Blair
John K. Blake
Dick Bobilin
Rodney J. Boehm
Steve Bootman
Jim Bradley
Hans Breuer
Robert Brooks
Paul Bryan
Bill Buckley
James P. Burkitt
Dennis Burroughs
Dave Buster
Steven Byars
David R. Cairns
Larry Campbell
L.E. Cantwell
J. Martin Carroll
Jack Caulder
V.V. Chalam
Jim Chamberlin
Lynn Chapman
Judy Chavel

NAME OF REPRESENTATIVE

S.J. Chen
Yau Ching
Dick H. Chiu
DooWhan Choi
George Chow
Robert W. Cubbage
Duane Cunningham
Grant Cyboron
James Dahl
R.P. Dave
P.F. DeDuck
Lucian V. Deas
Oscar Del Rio
Tom Dixon
Mounia Doukkapi
Thomas Eames
John Eaves
Dennis Edinger
Gustaf Ehrner
J.L. Eitel
John Ellson
Carl Engineer
Bill Erickson
David Evans
John Fahy
Ron Fang
L.A. Ferrara
Dick Fish
Gary Fishman
Jeffrey L. Foust
John W. Fox
Thomas A. Gajeski
Roselyne Genin
Suvankar Ghosh
Harold Goodnight
Steven Gorshe
Maynard A. Graden III
Edward P. Greene
C. George Griffith
Lori Gummerus
David Hanna
Bernard Harris
Ken Hartin
Eileen M. Healy
Thomas R. Helmes
Clive Holborow
Nian-Ciyi Huang

NAME OF REPRESENTATIVE

Charles E. Huffman
John Hughes
Raju Iyer
Al Jacobsen
Joel E. Jakubson
W.W. Janssen
Myron Jeffries
Phillip Johnson
Liz Jou
David Jurling
Ullas Kamath
Tetsuya Kanada
Leo Katz
Liba Khairandish
Danny Kimbrough
Frank Klopfer
Ed Knapp
Demosthenes J. Kostas
Lowell G. Krandell
Shinya Kukita
Angela LaSell
Bengt Lagerstedt
Richard Lau
Gosta Leijonhufrud
Damien Lemay
Steven L. Levine
Ben Levitan
Stephen Linskey
Kuo-Hui Liu
Russell B. Lloyd
Lawrence A. Marshall
Rick Masloski
Frank McAllum
John J. McDonough
James McEachern
Rick McNealy
Ricardo Mediavilla
Joe Mendoza
Daniel Millicker
Tom Moore
Mike Nawrocki
Rick Nickells
Greg Nulty
Dennis O'Donohue
Peter I. Obasuyi
Richard L. Odenweller
Roger Pandanda

NAME OF REPRESENTATIVE	
Corey M. Parollina	
Rockie Paslucci	
Dave W. Payne	
Eduardo Paz	
Kevin Pickles	
Frank Principe	
Walter Proebste	
Farooq Raza	
Andy Reid	
Barrett Robb	
Martin Roberts	
W. Foy Robinson	
Ted Ronley	
Fred Saal	
Sanjiv Saha	
Sabit Say	
M.G. Schachtman	
John Schembri	
Brian Schoenherr	
Carl Sealock	
Amitabha Sen	
Mike Sexton	
Rand Sherman	
Vishnu Shukla	
Frans Siebelink	
Ted Sirrs	
Torbjorn Skarsgard	
Barbara Engel Smith	
Mark J. Soulliere	
John Spiller	
Craig Stary	
Dick Stom	
Mark Sucharczuk	
Hideo Sugihara	
Richard Sun	
Steven Tabaska	
Jacques Tamisier	
Terdtoon Tapjan	
Linda Taylor	
Greg Theus	
John Thielen	
T.D. Timmons	
Norman Toms	
Earl Turner	
Everett J. Turvey	
Hiromi Ueda	
Victor A. Vachhani	

NAME OF REPRESENTATIVE

Eve Varma
Michael E. Varrassi
Ben Wagner
Steven C. Wainz
R.E. Weadon
Terry White
Clark E. Woodward III
Tim Wright
William Wuu
Fu-Chin Yang
Paul Yang
Yoshi Yokoyama
Robert T. Zader

AMERICAN NATIONAL STANDARD FOR TELECOMMUNICATIONS DIGITAL HIERARCHY OPTICAL INTERFACE RATES AND FORMATS SPECIFICATIONS

CONTENTS

FIGURES

TABLES

APPENDIXES

1. Scope

This document describes a base rate and format along with a multiplexing scheme which will result in a modular family of rates and formats available for use in optical interfaces. Other issues include layering of overhead, definitions of function and position of overhead, frequency justification at terminals, scrambling, and standardized loading of different payloads into the transport frame. It does not include the specification of optical interface parameters (see Reference [1]). References to related standards documents and activities are provided. It is always assumed that when the signal described herein is transmitted, it is directly converted to light pulses according to Reference [1]. It is not intended that this standard serve as an electrical interface specification.

2. Referenced Publications

This standard is intended to be used in conjunction with the following American National Standards for Telecommunications.

[1] Proposed American National Standard for Telecommunications Digital Hierarchy Optical Interface Specifications: Single-Mode, T1X1.4/87-014R4.

[2] American National Standard for Telecommunications - Synchronization Interface Standards for Digital Networks, ANSI T1.101-1987.

[3] American National Standard for Telecommunications Digital Hierarchy Electrical Interfaces, ANSI T1.102-1987.

[4] American National Standard for Telecommunications Digital Hierarchy Synchronous DS3 Format Specification, ANSI T1.103-1987. (Commonly referred to as SYNTRAN.)

[5] Proposed American National Standard for Telecommunications - Functional Requirements for Fiber Optic Terminating Equipment, T1M1.2/87-037R2.

[6] Proposed American National Standard for Telecommunications - Operations, Administration, Maintenance, and Provisioning - Lower Layer Protocols for Interfaces between Operations Systems and Network Elements, T1M1.5/87-021.

[7] Proposed American National Standard for Telecommunications Digital Hierarchy Formats Specifications, T1X1.4/87-702R4.

3. Abbreviations

AIS	- Alarm Indication Signal
APS	- Automatic Protection Switching
BER	- Bit Error Ratio
BIP-N	- Bit Interleaved Parity - N
CAS	- Channel Associated Signaling
EOC	- Embedded Operations Channels
FEBE	- Far End Block Error
FERF	- Far End Receive Failure
LLDL	- Low Level Data Link

LTE	- Line Terminating Equipment
NDF	- New Data Flag
NE	- Network Element
OC-1	- Optical Carrier level 1
OC-N	- Optical Carrier level N
OS	- Operation System
POH	- Path Overhead
PTE	- Path Terminating Equipment
SPE	- Synchronous Payload Envelope
STE	- Section Terminating Equipment
STS	- Synchronous Transport Signal
STS-1	- Synchronous Transport Signal level 1
STS-N	- Synchronous Transport Signal level N
STS-Nc	- Concatenated Synchronous Transport Signal level N
VT	- Virtual Tributary
VTx	- VT of size "x" (currently x = 1.5, 2, 3 or 6)
VTx-Nc	- Concatenated Virtual Tributary

4. Definitions

Alarm Indication Signal (AIS) - A code sent downstream in a digital network as an indication that an upstream failure has been detected and alarmed. It is associated with multiple transport layers as shown in Figure 30.

Bit Interleaved Parity - N (BIP-N) - A method of error monitoring. If even parity is used, an N bit code is generated by the transmitting equipment over a specified portion of the signal in such a manner that the first bit of the code provides even parity over the first bit of all N-bit sequences in the covered portion of the signal, the second bit provides even parity over the second bits of all N-bit sequences within the specified portion, etc. Even parity is generated by setting the BIP-N bits so that there are an even number of 1s in each of all N-bit sequences including the BIP-N.

Concatenated Synchronous Transport Signal level N (STS-Nc) - An STS-N Line layer signal in which the STS Envelope Capacities from the N STS-1s have been combined to carry an STS-Nc Synchronous Payload Envelope (SPE) which must be transported not as several separate signals but as a single entity.

Concatenated Virtual Tributary (VTx-Nc) - A set of Virtual Tributaries (VTs) in which the VT Envelope Capacities from N VTxs have been combined to carry a VTx-Nc which must be transported not as several separate signals but as a single entity. (Currently applies only to VT6-1 as described in Section 10.2.6).

DS0 Path Terminating Equipment (DS0 PTE) - Network elements which multiplex demultiplex the DS0 channels. DS0 PTEs originate, access, modify and/or terminate the DS0 signaling information necessary to transport the DS0 channels.

Far End Block Error (FEBE) - An indication returned to a source transmitting node that an errored block has been detected at the sink receiving node.

Fixed Stuff (R bits and bytes) - Fixed stuff (R) bits and bytes are used to compensate for the differences between the bandwidth available in the STS-1 and VT Synchronous Payload Envelopes and the bandwidth required for the actual payload mappings (i.e., DS1, DS1C, DS2, DS3, etc.). They are defined to facilitate easy interworking with existing transmission systems or to allow easy interworking between fixed and floating VTs. R bits and bytes have no defined value. The receiver is required to ignore the value of these bits/bytes.

Line - A transmission medium, together with the associated equipment, required to provide the means of transporting information between two consecutive Network Elements (NEs) one of which originates the line signal and the other terminates the line signal. See Figure 1 and Figure 2.

Line Alarm Indication Signal (AIS) Code - A Line AIS code is generated by a regenerator upon loss of input signal or loss of frame. The Line AIS signal will maintain operation of the downstream regenerators and therefore prevent generation of unnecessary alarms. At the same time, data and orderwire communication is retained between the regenerators and the downstream Line Terminating Equipment (LTE).

Line Far End Receive Failure (FERF) - An indication returned to a transmitting Line Terminating Equipment (LTE) upon receipt of a Line AIS code or detection of an incoming line failure at the receiving LTE.

Line Terminating Equipment (LTE) - Network elements which originate and/or terminate line (OC-N) signals. See Figure 1 and Figure 2. LTEs originate, access, modify and/or terminate the transport overhead.

Most Significant Bit - The left-most bit position. Bit 1 as illustrated in Figure 3.

Optical Carrier level 1 (OC-1) - The optical signal that results from an optical conversion of an STS-1 signal. It is this signal that will form the basis of the interface.

Optical Carrier level N (OC-N) - The optical signal that results from an optical conversion of an STS-N signal.

Path - A path at a given rate is a logical connection between the point at which a standard frame format for the signal at the given rate is assembled, and the point at which the standard frame format for the signal is disassembled. See Figure 1 and Figure 2.

Path Overhead (POH) - Overhead assigned to and transported with the payload until the payload is demultiplexed. It is used for functions that are necessary to transport the payload.

Payload Pointer - The pointer that indicates the location of the beginning of the Synchronous Payload Envelope.

Section - The portion of a transmission facility, including terminating points, between (i) a terminal Network Element (NE) and a regenerator or (ii) two regenerators. A terminating point is the point after signal regeneration at which performance monitoring is (or may be) done. See Figure 1 and Figure 2.

STS Envelope Capacity - Bandwidth within, and aligned to the STS Frame which carries the STS Synchronous Payload Envelope (SPE). This bandwidth can be combined from N STS-1s in order to carry an STS-Nc SPE.

STS Path Overhead (STS POH) - Nine evenly distributed Path Overhead bytes per 125 microseconds starting at the first byte of the STS SPE. STS Path Overhead provides for communication between the point of creation of an STS SPE, and its point of disassembly. STS Path Overhead is described in Section 9.2.3.

STS Path Terminating Equipment (STS PTE) - Network Elements which multiplex/demultiplex the STS payload. STS PTEs originate, access, modify and/or terminate the STS Path Overhead necessary to transport the STS payload.

STS Payload Capacity - The maximum bandwidth within the STS Synchronous Payload Envelope that is available for payload.

STS Synchronous Payload Envelope (STS SPE) - A 125 microsecond frame structure composed of STS Path Overhead and bandwidth for payload. The term generically refers to STS-1 SPEs and STS-Nc SPEs which are described in Sections 8.1.2 and 8.3 respectively.

Super Rate Signals - A signal that has to be carried by a Concatenated Synchronous Transport Signal level Nc (STS-Nc).

Synchronous - The essential characteristic of time-scales or signals such that their corresponding significant instants occur at precisely the same average rate.

Synchronous network - The synchronization of synchronous transmission systems with synchronous payloads to a master (network) clock which can be traced to a reference clock.

Synchronous payloads - Payloads derivable from a network transmission signal by removing integral numbers of bits in every frame, i.e. there are no variable bit stuffing rate adjustments required to fit the payload in the transmission signal.

Synchronous Transport Signal level 1 (STS-1) - The basic logical building block signal with a rate of 51.840 Mbit/s. No electrical interface is defined in this document.

Synchronous Transport Signal level N (STS-N) - This signal is obtained by byte interleaving N STS-1 signals together. The rate of the STS-N is N times 51.840 Mbit/s.

Transport - Facilities associated with the carriage of OC-1 or higher level signals.

Transport Overhead - The overhead added to the STS SPE for transport purposes. Transport Overhead consists of Line and Section Overhead. See Section 8.

Unassigned (X) Bits/Bytes - Those locations within the signal that have not had a function or value assigned to them at this time. The receiver is required to ignore the value of these bytes.

Unequipped channel - A portion of an STS-N such as an STS-1 SPE or VT SPE that is intentionally unoccupied.

Unequipped Indication - A code placed in unequipped channels by originating equipment to indicate to Path Terminating Equipment that the channel is intentionally unoccupied.so that alarms can be inhibited.

User channel - This is allocated to the user for input of information such as data communication for use in maintenance activities and remoting of alarms external to the span equipment in a proprietary fashion.

Virtual Tributary (VT) - A structure designed for transport and switching of sub-STS-1 payloads. There are currently four sizes of VT as defined in Section 8.1.3.

VT Envelope Capacity - Bandwidth within, and aligned to, the VT Superframe that is available for the VT Synchronous Payload Envelope.

VT Group - A 9 row by 12 column structure (108 bytes) that carries one or more VTs of the same size. Seven VT groups (756 bytes) are byte interleaved within the VT-organized SPE.

VT Path Overhead (VS) - One Path Overhead byte per 500 microseconds located at the first byte of the VT SPE. VT Path Overhead provides for communication between the point of creation of a VT SPE, and its point of disassembly. VT Path Overhead is described in Section 9.3.

VT Path Terminating Equipment (VT PTE) - Network elements which multiplex/demultiplex the VT payload. PTEs originate access, modify and/or terminate the VT Path Overhead necessary to transport the VT payload.

VT Payload Capacity - The maximum bandwidth within the VT Synchronous Payload Envelope that is available for payload.

VT Superframe - The VT is organized into a 500 microsecond superframe structure overlaid on and aligned to the 125 microsecond STS-1 Synchronous Payload Envelope (SPE). Contained within this structure is the VT Payload Pointer and the VT SPE.

VT Synchronous Payload Envelope (VT SPE)- A 500 microsecond frame structure carried by the VT composed of VT Path Overhead (POH) and bandwidth for payload. The envelope is contained within, and can have any alignment with respect to, the VT Envelope Capacity. The term generically refers to VT1.5, VT2, VT3, VT6, and VTx-Nc SPEs which are described in Section 8.1.3.

VTx - A VT of size "x" (currently x = 1.5, 2, 3 or 6).

5. General

A primary goal in creating this standard for the rates and formats for optical interfaces is to define a synchronous optical hierarchy with sufficient flexibility to carry many different capacity signals. This has been accomplished by defining a basic signal of 51.840 Mbit/s and a byte interleaved multiplex scheme which results in a family of standard rates and formats defined at a rate of N times 51.840 Mbit/s, where N is an integer. Presently, the maximum value of N is 255.[1] Since some signals which need to be transported are greater than the basic rate defined (such as the broadband ISDN and the 139.264 Mbit/s signals) a technique of linking several basic signals together to build a transport signal of varying capacity has also been defined.

The basic signal can be divided into a portion assigned for Transport Overhead and a portion which contains the payload. This payload can be used to transport DS3 signals or to transport a variety of sub-DS3 signals. To maintain a consistent payload structure while providing for transport of a variety of lower rate services (such as DS1, DS1C, DS2 or 2.048 Mbit/s signals), a structure called a Virtual Tributary (VT) has been defined. This structure is designed to facilitate consistent transport and switching of various payloads uniformly by handling only VTs. All services below the DS3 rate are transported within a VT structure.

---

1. The maximum value of N is limited by the specification of the STS-1 ID (see section 9) as one byte. The value of 0 is not used.

Many different types of overhead have been defined, including overhead for maintenance, user channels, frequency justification, orderwire, channel identification, and growth channels. A layered approach to overhead has been established whereby overhead bandwidth has been allocated to a layer based on the function addressed by that particular channel. This layered approach, detailed in Section 9, allows creation of equipment which needs not access all layers of overhead thereby allowing the creation of equipment to meet different needs. Growth channels have been identified to allow for future uses not defined or conceived at this time.

The rest of the document concentrates on the actual specification of the rates and formats for optical interfaces. Section 6 describes the rates while Section 7 covers timing and synchronization issues. Section 8 covers the frame formats for the base signal as well as higher rate signals. Overhead functions as well as layering of the overhead are described in Section 9. Payload Pointers for STS-1 and Virtual Tributary processing are described in Section 10. Multiplexing procedures are outlined in Section 11 and the different payload mappings defined thus far are detailed in Section 12. Automatic Protection Switching functions are described in Section 13 and Data Communications Channel requirements are provided in Section 14. It is anticipated that this document will be revised as new signals are defined that need to be transported.

6. Rates

6.1 STS-1/OC-1 Rate

The basic modular signal shall be termed the "Synchronous Transport Signal level 1", or STS-1. The rate is 51.840 Mbit/s. The optical counterpart of the STS-1 is the Optical Carrier - Level 1 signal, OC-1, which is the result of a direct optical conversion of the STS-1 after frame synchronous scrambling (see section 11.3).

6.2 Synchronous Hierarchical Rates

The definition of the first level (STS-1, OC-1) defines the entire hierarchy of synchronous optical signals, since the higher level signals are obtained by synchronously multiplexing lower level signals. The higher level signals are denoted by STS-N and OC-N where N is an integer.

There is an integer multiple relationship between the rates of the basic module OC-1 and the multiplexed signal OC-N, i.e. the rate of OC-N is equal to N times the rate of OC-1.

In the range from 1 to 48, this standard recognizes only certain values of N. These values of N are 1, 3, 9, 12, 18, 24, 36 and 48. Table 1 lists standard Optical Carrier (OC) rates from 51.84 Mbit/s up through 2488.32 Mb/s. Values of N greater than 48 will be addressed in the future.

7. Timing and Synchronization

All synchronous optical network elements shall be integrated into the synchronization hierarchy as described and specified in Reference [2]. The clocks used to synchronize these network elements shall be stratum 3 or better quality. In addition, the short term stability of the associated external clock or internal clock must meet the provisional requirements given in Figure 4. The internal oscillator(s) must have a minimum accuracy of ±20 ppm in order to generate proper maintenance signals. Timing and Synchronization Application Guidelines are contained in Appendix A.

8. Transport Formats

8.1 Frame Structure Of The STS-1

The STS-1 frame depicted in Figure 5 consists of 90 columns and 9 rows of 8-bit bytes, for a total of 810 bytes (6480 bits).[2] With a frame length of 125 microseconds (i.e., 8000 frames per second), the STS-1 has a bit rate of 51.840 Mbit/s. The order of transmission of bytes is row by row, from left to right. In each byte, the most significant bit is transmitted first (see Figure 3).

8.1.1 Transport Overhead

Referring to Figure 5, the first three columns are the Transport Overhead, which contains overhead bytes for Section and Line layers. Twenty-seven bytes have been assigned, with nine bytes for Section Overhead and eighteen bytes for Line Overhead. Details of these overhead allocations are described in Section 9.

8.1.2 STS-1 Synchronous Payload Envelope

The STS-1 Synchronous Payload Envelope (SPE) is depicted in Figures 6, 7, and 8. It consists of 87 columns and 9 rows of bytes, for a total of 783 bytes as illustrated in Figure 6. Column 1 contains the STS Path Overhead (9 bytes) and the remainder (774 bytes) is available for payload as illustrated in Figure 7.

The STS-1 SPE may begin anywhere in the STS Envelope Capacity illustrated in Figure 8. Typically it begins in one frame and ends in the next (although it may be wholly contained in one frame). The payload pointer contained in the Transport Overhead designates the location of the byte where the STS-1 SPE begins. STS-1 Payload Pointers are discussed in Section 10.2.

STS Path Overhead is defined in each payload and is to be used to communicate functions from the point where a service is mapped into the STS SPE to where it is delivered. STS Path Overhead is discussed in detail in Section 9.

8.1.3 Virtual Tributary (VT) Structure

The Virtual Tributary is a structure designed for transport and switching of sub-STS-1 payloads. There are four sizes of VT: the VT1.5 (1.728 Mbit/s), the VT2 (2.304 Mbit/s), the VT3 (3.456 Mb/s), and the VT6 (6.912 Mb/s). These are illustrated in Figure 9. In the 9-row structure of the STS-1 Synchronous Payload Envelope, these VTs occupy 3 columns, 4 columns, 6 columns and 12 columns respectively.

In order to accommodate mixes of these VTs in an efficient manner, the VT-structured STS-1 SPE is divided into 7 VT Groups as illustrated in Figure 10. Each VT Group occupies 12 columns of the 9-row structure and may contain 4 VT1.5s, 3 VT2s, 2 VT3s or 1 VT6. Note that a VT Group must contain only one size of VT, however, each VT Group within an STS-1 may contain a different VT size. Figure 11 is a 3 dimensional representation of the STS-1 SPE which further illustrates this point.

In Figures 12, 14, 16 and 18, the entire STS-1 SPE is shown containing one of the four VT sizes. Figures 13, 15, 17 and 19 define the relationship between the VT number, VT Group number and column number in the STS-1 SPE from Figures 12, 14, 16 and 18 respectively. The "Byte 1" references in these figures refer to the first byte of the VT as defined in Figure 9.

---

2. Byte and Octet are synonymous.

There are two possible modes of operation of the VT structure: Locked and Floating. Locked mode minimizes interface complexity in distributed 64 kbit/s switching; Floating mode minimizes delay for distributed VT switching.

8.1.3.1 Floating VT Mode

In the floating VT mode, four consecutive 125 microsecond frames of the STS-1 SPE are organized into a 500 microsecond superframe, the phase of which is indicated by the Multiframe Indicator byte (H4) in the STS Path Overhead. This defines a 500 microsecond structure for each of the VTs called the VT Superframe. The VT Superframe contains the VT Payload Pointer and the VT Synchronous Payload Envelope as shown in Figure 20. The VT Pointer occupies 4 bytes: V1, V2, V3 and V4, and the remaining bytes define the VT Envelope Capacity which is different for each VT size. The placement of the V1-V4 bytes is such that they will appear in Byte 1 of the VT, regardless of the VT size.

Figure 21 illustrates the four VT SPEs corresponding to the four VT sizes. Each VT SPE contains one byte of VT Path Overhead (V5) and the remaining bytes define the VT Payload Capacity which is different for each VT size.

The VT Payload Pointer provides for flexible and dynamic alignment of the VT SPE within the VT Envelope Capacity, independent of other VT SPEs. VT Payload Pointers are further described in Section 10.2.

Sub-STS-1 payloads that require capacity greater than a VT6 are accommodated by concatenating N VT6s into a VT6-Nc. The VT6-Nc SPE is illustrated in Figure 22. Since N VT Payload Pointers will be associated with this one envelope, a concatenation indication is included in the pointer definition to signify their relationship. Currently, the N VT6s in a VT6-Nc must be contiguous and wholly contained within an STS-1 SPE.

8.1.3.2 Locked VT Mode

Locked VT Mode of transport is a fixed mapping of synchronous VT structured payloads into a STS-1 SPE. This provides a direct correspondence between subtending tributary information and the location of that information within the STS-1 SPE. Since the tributary information is fixed and immediately identifiable with respect to the STS-1 Pointer, all 108 bytes of a VT Group are available for payload usage.

Figure 23 illustrates the conversion from Floating and Locked VT modes for each of the four VT sizes. Note that certain bytes (R) in the current set of mappings are not used in order that those mappings can be used in both locked and floating modes. Since the V1-V4 and V5 bytes are reserved, the 500 microsecond VT superframe is unnecessary. Therefore, the role of the Multiframe Indicator byte (H4) in this mode is to define 2 and 3 millisecond superframes for DS0 signaling. Payload mappings which use this mode are further described in Section 12.

8.2 Frame Structure of The STS-N

The STS-N signal is formed by byte interleaving N STS-1 signals. The STS-N frame structure is depicted in Figure 24. The transport overhead channels of the individual STS-1 signals must be frame aligned before interleaving. The associated STS SPEs are not required to be aligned because each STS-1 will have a unique payload pointer to indicate the location of the SPE.

When forming the STS-N frame, as noted in Sections 9.2.1 and 9.2.2, certain Section and Line Layer Overhead bytes in the STS-1#2 through #N are unspecified at this time. The receiver is required to ignore the value of these bytes.

8.3 Concatenated STS-1s

Super Rate Services are services which require multiples of the STS-1 rate, such as the broadband ISDN H4 channel. They are mapped into the STS-Nc SPE and transported as a concatenated STS-Nc whose constituent STS-1s are kept together. The STS-Nc is carried by an STS-M line signal where M≥N. The STS-Nc must be multiplexed, switched and transported through the network as a single entity. A concatenation indication, used to show that the STS-Nc should be kept together, is contained in the STS-1 payload pointer. The concatenation indication shall be a special value for the STS-1 pointer used in conjunction with the new data flag. Details of STS-1 concatenation are provided in Section 10 and mapping of super rate services is covered in Section 12.

The STS-Nc SPE is depicted in Figure 25. It consists of N x 87 columns and 9 rows of bytes. The order of transmission is row by row, from left to right.

Only one set of STS Path Overhead is required in the STS-Nc SPE. The STS-Nc SPE is carried within the STS-Nc such that the STS Path Overhead always appears in the first of the N STS-1s which make up the STS-Nc.

9. Layered Overhead and Transport Functions

The overhead and transport functions may be broken into layers to promote understanding and structure. In order of increasing complexity from the viewpoint of hardware and the optical interface frame format, the layers are Photonic, Section, Line and Path. The layers have a hierarchical relationship and can be considered either from the top down, or the bottom up. The top down approach is useful for providing a general introduction to the individual layers and their functionality. The following paragraph introduces the layers from the top down.

Each layer requires the services of all lower level layers to perform its own function. For example, suppose that two Path layer processes are exchanging DS3s. The DS3s plus Path overhead must be mapped into an STS-1 SPE which is then given to the Line Layer. The Line layer multiplexes several inputs from the Path layer (frame and frequency aligning each one) and adds Line overhead (e.g. overhead required for protection switching). Finally, the Section layer provides framing and scrambling prior to optical transmission by the Photonic layer.

The bottom up approach to the layers is useful for describing the system hardware partitioning as well as the evolution of the optical interface format. The following paragraph introduces the layers from the bottom up.

Each layer builds on the services provided by the lower layer. The Photonic layer provides optical transmission at some bit rate, the Section layer provides framing and scrambling for the bits being transmitted, the Line layer provides Line maintenance and protection as well as multiplexing of STS-1 channels, the Path layer provides a mapping function from various services into the STS-1 SPE format. Note that all layers can be implemented at one time or they can be broken into separate steps.

9.1 Optical Interface Layers

The following sections describe each layer in detail. Each description includes a broad classification of the layer followed by a specification of the main functions it provides. Finally, examples of system hardware associated with the layers are given in order to clarify the role it plays. The relationship of the layers to each other is depicted in Figure 26.

9.1.1 Photonic Layer

The Photonic layer deals with the transport of bits across the physical medium. No overhead is associated with the Photonic Layer.

The main function of this layer is conversion between STS signals and OC signals. Issues dealt with at this layer include optical pulse shape, power levels and wavelength. Specification for these are contained in American National Standard for Telecommunications Digital Hierarchy Optical Interface Specifications: Single-Mode." (See Reference [1]).

Electro-optical units communicate at this level.

9.1.2 Section Layer

The Section layer deals with the transport of an STS-N frame across the physical medium. See Figures 1 and 2. This layer uses the Photonic layer to form the physical transport.

Functions in this layer include framing, scrambling, section error monitoring and communicating Section level overhead (such as local order wire). The overhead defined for this layer is read, interpreted and/or modified by all equipment which terminates this layer.

Note that the Section and Photonic layers can be utilized in some equipment without the higher layers. The OC-N regenerator is an example of where this could occur.

9.1.3 Line Layer

The Line layer deals with the reliable transport of Path layer payload and its overhead across the physical medium. See Figures 1 and 2. Overhead added here is accessed at points where STS-N signals are formed or terminated. All lower layers exist to provide transport for this layer.

The main functions of this layer are to provide synchronization and multiplexing for the Path layer. The overhead associated with these functions include overhead for maintenance and protection purposes and is inserted into the Line overhead channels. The overhead defined for this layer is read, interpreted and/or modified by all equipment which terminates this layer.

An example of system equipment which communicates at this level is an OC-N OC-M multiplexer.

9.1.4 Path Layer

The Path layer deals with the transport of services between Path Terminating Equipment (PTE). See Figures 1 and 2. Examples of such services are DS1s, DS3s (synchronous and asynchronous), DS4NAs, Video signals, etc.

The main function of the Path layer is to map the services into the format required by the Line layer. In addition, this layer communicates end to end via the Path overhead. The overhead defined for this layer is read, interpreted and/or modified by all equipment which terminates this layer.

An example of system equipment which communicates at this level is DS3 to STS-1 mapping circuits.

9.1.5 Interaction of the Layers

The interaction of the optical interface layers are depicted in Figure 26. These will be described in a top down approach. Note that each layer:

1. communicates (horizontally) to peer equipment in that layer, and
2. processes certain information and hands it (vertically) to the next layer

The interactions will be described in terms of each level's horizontal and vertical transactions.

Following a top down approach, the figure shows network services (DS1s, DS3s, DS4NAs, etc.) as inputs to the Path layer. This layer transmits (horizontally) to its peer entities the services and the Path layer overhead. The Path layer maps the services and Path overhead into SPEs which it hands (vertically) to the Line layer.

The Line layer transmits to its peer entities SPEs and also the Line layer overhead. It maps the SPEs and Line overhead into STS-N signals (at this time payload justifications and multiplexing occur) and hands them to the Section layer.

The Section layer transmits to its peer entities STS-N signals and Section layer overhead (e.g. local orderwire). It maps STS-Ns and the Section overhead into pulses which are handed to the Photonic layer which transmits optical pulses to its peer entities.

Note that all four layers may not be used in certain pieces of equipment. For example, an OC-N regenerator would use only the first two layers (Photonic and Section). Also, a terminal which merely routes its SPEs and does not accept any new inputs (from the Path layer) only uses the first three layers (Photonic, Section and Line).

9.2 STS-1 Overhead Descriptions

Figure 27 illustrates the location of the overhead bytes in the STS-1 frame. The functions assigned to the Section and Line layers have been combined into a structure of 27 bytes called the transport overhead which occupy the first three columns of the frame. The functions of the Path layer have been assigned 9 bytes in the first column of the STS SPE. This distinction is made so that transmission equipment can be specified without regard to the information structure that is being transported.

Each of the overhead bytes is defined in this section and is assigned to a layer and position in the frame (refer to Figure 27). Data links that are defined are for use by the transmission equipment for transmitting messages, commands and alarms associated with transmission functions. Examples include protection switching and fault isolation procedures. Care has been taken to define messages in each channel to minimize the number of messages that need to be passed between layers. For example, the protection switching messages will be all contained in the protection switching channel and will not need to be communicated to equipment that is only operating at other layers.

Note that in all cases the overhead associated with a given layer is read, interpreted and/or modified by the equipment terminating that layer. Thus it must be recreated prior to insertion on the outgoing signal, rather than being regenerated unchanged.

The descriptions will start with the Section layer since there is no overhead associated with the Photonic layer.

9.2.1 Section Overhead

Framing (A1, A2) - Two bytes are dedicated to each STS-1. The pattern shall be F628 Hex (1111011000101000). These bytes shall be provided in all STS-1 signals within an STS-N signal.

STS-1 Identification (STS-1 ID)(C1) - This is a unique number assigned just prior to byte interleaving that stays with that STS-1 until deinterleaving. This is normally accomplished in Line Terminating equipment. This can be used in the framing and deinterleaving process to determine the position of the other signals. The C1 byte in each STS-1 shall be set to a binary number corresponding to its order of appearance in the byte interleaved STS-N frame. The first STS-1 to appear in the frame shall be designated #1 (00000001). This byte shall be provided in all STS-1 signals within an STS-N signal.

Section BIP-8 (B1) - One byte is allocated in each STS-1 for a section error monitoring function. This function shall be a bit interleaved parity 8 code using even parity. The section BIP-8 is calculated over all bits of the previous STS-N frame after scrambling. The computed BIP-8 is placed in the B1 byte of STS-1 #1 before scrambling. This byte is defined only for STS-1 #1 of an STS-N signal.

Orderwire (E1) - One byte is allocated to be used as a local orderwire channel which shall be used as a voice communication channel. It is reserved for communication between regenerators, hubs and remote terminal locations. Orderwire specifications are provided in Reference [5]. It is defined only for STS-1 #1 of an STS-N signal.

Section User Channel (F1) - A byte is set aside for the user's purposes. This byte shall be passed from one section level entity to another and shall be terminated at all section level equipment. This byte is defined only for STS-1 #1 of an STS-N signal.

Section Data Communication Channel (Data Com) (D1, D2, D3) - Three bytes are allocated for Section data communication and should be considered one 192 kbit/s message based channel for alarms, maintenance, control, monitor, administration and other communication needs between Section terminating equipment. This is available for internally generated, externally generated, and manufacturer specific messages. These bytes are defined only for STS-1 #1 of an STS-N signal.

9.2.2 Line Overhead

Pointer (H1, H2) - Two bytes are allocated to a pointer which indicates the offset in bytes between the pointer and the first byte of the STS SPE. It shall be used to align the STS-1 Transport Overheads in an STS-N signal as well as perform frequency justification. These bytes shall be provided in all STS-1 signals within an STS-N signal.

Pointer Action Byte (H3) - The pointer action byte is allocated for frequency justification purposes. Depending on the pointer value this byte is used to adjust the fill of input buffers. In the event of a negative justification, it carries valid information. This byte shall be provided in all STS-1 signals within an STS-N signal. The value contained in this byte when not used to carry valid information is not defined. The receiver is required to ignore the value contained in this byte whenever it is not used to carry valid information.

Line BIP-8 (B2) - One byte is allocated in each STS-1 for a line error monitoring function. This function shall be a bit interleaved parity 8 code using even parity. The Line BIP-8 is calculated over all bits of the Line Overhead and STS-1 Envelope Capacity of the previous STS-1 frame before scrambling. The computed BIP-8 is placed in the B2 byte of the STS-1 before scrambling. This byte shall be provided in all STS-1 signals within an STS-N signal.

APS Channel (K1, K2) - Two bytes are allocated for Automatic Protection Switching (APS) signaling between Line level entities. These bytes are defined only for STS-1 #1 of an STS-N signal.

Line Data Communication Channel (Data Com)(D4-D12) - Nine bytes are allocated for Line data communication and should be considered one 576 kbit/s message based channel for alarms, maintenance, control, monitor, administration and other communication needs between Line terminating entities. This is available for internally generated, externally generated, and manufacturer specific messages. These bytes are defined only for STS-1 #1 of an STS-N signal.

Growth (Z1, Z2) - Two bytes are set aside for functions not yet defined. These bytes have no defined value. The receiver is required to ignore the value contained in these bytes. These bytes are reserved in all STS-1s of an STS-N.

Orderwire (E2) - One byte is allocated in this layer for an express orderwire between Line entities. Orderwire specifications are provided in Reference [5]. This byte is defined only for STS-1 #1 of an STS-N signal.

9.2.3 STS Path Overhead

The STS Path Overhead (STS POH) will be assigned to and remain with the payload until the payload is demultiplexed and will be used for functions that are necessary in transporting all STS Synchronous Payload Envelopes (STS SPEs). In the case of a Super Rate Service only one set of path overhead is required and is contained in the first STS-1 of the STS-Nc. (See Section 8.3). Note that this does not preclude the allocation of other overhead in specific mappings (such as stuff control for mapping asynchronous DS3) which is payload specific whereas the overhead defined in this section is payload independent.

STS Path Trace (J1) - This byte is used to repetitively transmit a 64 byte, fixed length, string so that a Path receiving terminal can verify its continued connection to the intended transmitter. The content of the message is not constrained by this standard since it is assumed to be user programmable at both transmit and receive ends. However, it is suggested that a 64 by 8 bit ASCII Common Language Location Identifier (CLLI) code, padded with NULL characters and terminated with CR/LF, would be a suitable trace message. If no message has been loaded then 64 NULL characters (Hex 00) shall be transmitted.

Path BIP-8 (B3) - One byte is allocated for a path error monitoring function. This function shall be a bit interleaved parity 8 code using even parity. The path BIP-8 is calculated over all bits of the previous STS SPE before scrambling.

STS Path Signal Label (C2) - One byte is allocated to indicate the construction of the STS SPE. Of the 256 possible binary values, 3 are defined here and the remaining 253 codes are reserved to be defined as required in specific STS payload mappings:

- Code 0 indicates "STS SPE Unequipped." This code shall be originated if the Line Connection is complete but there is no Path originating equipment.
- Code 255 (all '1's) indicates "STS Path Alarm Indication Signal". This code shall be originated if the Line connection is incomplete.
- Code 1 indicates "STS SPE Equipped - Non Specific Payload". This code can be used for all payloads that need no further differentiation, or that achieve differentiation by other means such as messages from an OS.

Note that any code received, other than codes 0 or 255, constitutes an "Equipped" condition.

Path Status (G1) - One byte is allocated to convey back to an originating STS PTE the path terminating status and performance. This feature permits the status and performance of the complete duplex path to be monitored at either end, or at any point along that path. As illustrated in Figure 28, Bits 1 through 4 convey the count of interleaved- bit blocks that have been detected in error by the Path BIP-8 code (B3). This count has 9 legal values, namely 0...8 errors. The remaining 7 possible values represented by these 4 bits can only result from some condition unrelated to the forward path and shall be interpreted as zero errors. Bit 5 is an STS Path Yellow Indicator (see Section 9.4.3.2). Bits 6, 7 and 8 are unassigned at this time.

Path User Channel (F2) - One byte is allocated for user communication purposes between Path elements.

VT Multiframe Indicator (H4) - This byte provides a generalized multiframe indicator for payloads. Currently, this indicator is only used for VT structured payloads as described in Section 10.2.2.

Growth (Z3-Z5) - Three bytes are allocated for future as yet undefined purposes. These bytes have no defined value. The receiver is required to ignore the value contained in these bytes.

9.3 VT Path Overhead (V5)

There is one byte of VT Path Overhead in the first byte of a VT SPE or a VTx-Nc SPE (i.e., in the location pointed to by the VT Pointer), as shown in Figures 21 and 22.

This byte provides for VT Paths the same functions that B3, C2, and G1 provide for STS Paths, namely: Error checking, Signal Label, and Path Status.[3] The bit assignments of the VT Path Overhead are specified in the following paragraphs and are illustrated in Figure 29.

Bits 1 and 2 are used for error performance monitoring. A bit interleaved parity (BIP) scheme is specified. Bit 1 is set such that parity of all odd-numbered bits (1, 3, 5 and 7) in all bytes in the previous VT Synchronous Payload Envelope (SPE) is even, and bit 2 is set similarly for the even-numbered bits. Note that the calculation of the BIP-2 includes the VT Path Overhead bytes but excludes the VT Pointers.

Bit 3 is a VT Path Far-End-Block-Error (FEBE) indication that is sent back towards an originating VT PTE if one or more errors was detected by the BIP-2.

Bit 4 is unassigned (X). The receiver is required to ignore the value of this bit.

Bits 5 through 7 provide a VT Signal Label. 8 binary values are possible in these 3 bits. Similar to the STS Path Signal Label, code 0 indicates "VT Path Unequipped," code 7 indicates "VT Path AIS," and code 1 indicates "VT Path Equipped - Non Specific Payload." The remaining 5 codes are reserved to be defined as required in specific VT mappings. Any code received, other than 0 or 7, indicates an equipped VT Path.

Bit 8 is a VT Path Yellow indication (see Section 9.4.3.2).

V5 is used in floating VTs only and is designated as an R byte in Locked VTs.

9.4 Maintenance Signals

9.4.1 STS Maintenance Signals

9.4.1.1 STS SPE Unequipped Indication

The STS SPE Unequipped Indication is an all '0's STS Path Signal Label (after descrambling).

The code is generated as an all '0's STS Path Signal Label and a valid STS Path BIP-8 (B3); the remainder of the STS SPE is unspecified. A suggested code is all '0's STS SPE, which automatically results in a valid Path BIP-8 as well as the correct STS Path Signal Label; however, a receiver should not assume that an all '0's code was used.

9.4.1.2 Line AIS

Line Alarm Indication Signal (AIS) Code - The purpose of this code is to indicate to Line Terminating Equipment that a loss of signal condition of some type has been detected and alarmed at a regenerator (Section Terminating Equipment). A second function of the code is to provide a signal suitable for normal clock recovery at downstream regenerators and Line Terminating Equipment (a Keep Alive Signal).

Line AIS is detected as an all '1's in bits 6, 7 and 8 of the APS byte (K2) after descrambling.

---

3. VT Path Trace is for further study.

There are two alternative formats of Line AIS (at any given N); these two allow implementers the option of either full or partial scramblers in regenerators.

The first format, intended for implementations of regenerators that contain a full scrambler, is generated as: valid Section overhead and a scrambled all '1's pattern for the remainder of the signal resulting in a valid line BIP-8 (B2).

The second format, intended for implementations of regenerators that contain scramblers for Section overhead only, is generated as: valid Section Overhead, along with the specific code in Line Overhead byte locations K2 and B2 that results in an all '1's K2 byte and valid line BIP-8 when descrambled at the LTE, and an unscrambled alternating '10' sequence in the remainder of the Line Overhead and Envelope Capacity Locations.

9.4.1.3 Line Far End Receive Failure (FERF)

The purpose of this code is to return an indication to the transmitting LTE that the receiving LTE has detected an incoming line failure or is receiving Line AIS. Line FERF can be used to aid fault sectionalization.

Line FERF is detected by a '110' code in bit positions 6, 7, and 8 of the K2 APS byte after descrambling.

9.4.1.4 STS Path AIS

STS Path AIS is specified as an all '1's STS SPE after descrambling plus valid Line and Section Overhead. STS Path AIS is detected as an all '1's state of the STS Path Signal Label.

9.4.2 VT Maintenance Signals

9.4.2.1 VT SPE Unequipped Indication

VT Unequipped Indication is an all '0's VT Signal Label (after descrambling).

The code is generated as a valid VT Payload Pointer with an all '0's VT Signal Label (V5 Bits 5-7) and a valid VT Path BIP-2 (V5 Bits 1-2), the remainder of the VT SPE is unspecified. A suggested code is all '0's VT SPE, which automatically results in a valid BIP-2; however, a receiver should not assume that an all zeroes code was used.

9.4.2.2 VT Path AIS

VT Path AIS is specified as a valid VT Payload Pointer with all '1's code filling the VT Synchronous Payload Envelope. VT AIS is detected by observing '111' in the L1-L3 bits of the VT Path Overhead.

9.4.3 Applications of AIS and Yellow Signals

9.4.3.1 AIS

The Line and Path AIS may be represented by a layered model as shown in Figure 30. Equipment examples of how the various levels of AIS are generated and propagated in the network are illustrated in Figure 31.

When Section Terminating Equipment detects receipt of an invalid signal, it sends a Line AIS in the downstream direction.

When Line Terminating Equipment receives either an invalid signal or a Line AIS and is unable to protect the line, it sends an STS Path AIS downstream.

When STS Path Terminating Equipment receives either an invalid signal or an STS Path AIS, it propagates the appropriate AIS downstream. Figure 31 illustrates three cases: one where DS3 AIS is generated, one where a VT Path AIS is generated and one where a DS0 AIS is generated.

When VT Path Terminating Equipment receives either a VT Path AIS or an invalid signal, it generates the appropriate AIS downstream. Figure 31 illustrates two cases: one being a DS1 AIS and another being a DS0 AIS for elements that process DS0s. Signaling states for, and applications of, DS0 Path AIS require further study.

9.4.3.2 Yellow Signals

Yellow signals are applicable to the lowest maintainable facility level associated with a particular service. Upon detection of a service affecting failure at a terminal, a local Red alarm[4] is declared, and a Yellow signal is returned to the far end network element which terminates the service. Automatic service management processes are then initiated and maintained for the duration of the failure. Release from the alarm states and removal of the Yellow signal is coordinated between the source/sink network terminals to restore service.

Until recently, Yellow and Red alarm processes were limited to the DS1 facility level for simultaneous management (Carrier Failure Alarms/trunk conditioning) of all constituent DS0s. Transport of higher bandwidth services (e.g., video signals) has warranted studying DS3 based Red/Yellow alarm mechanisms. Furthermore, the direct DS0 mapping options in this standard (Section 12) and SYNTRAN have necessitated definition of a DS0 level Yellow signal.

Figure 31 illustrates Yellow signal originations. If future services are defined which are not dependent upon the existing DS1 or DS3 hierarchical levels for transport, there will be a need to provide VT and/or STS Path Yellow signaling between PTEs. In anticipation of such services, DS0, VT, and STS Path Terminating Equipment shall generate respective Yellow signals upon detection of an incoming failure or receipt of AIS. Until such services are identified and mappings specified, VT and STS Path Terminating Equipment shall have the option to ignore a received Yellow signal.

When DS0 Path Terminating Equipment receives either a DS0 Path AIS or an invalid signal, it generates a DS0 Path Yellow in the reverse direction and takes appropriate action locally to terminate the DS0 connection (e.g., trunk conditioning). Signaling states for, and applications of, DS0 Path Yellow require further study.

VT and STS Path Yellow signaling bit positions are shown in Figures 28 and 29. As shown in Figure 30, Yellow signals are only transmitted and received between peer layers. Receipt of a Yellow signal at a VT or STS path terminal does not result in the generation of a higher layer (lower bandwidth) Yellow signal. Note that the STS/VT Path Yellow indicators are not applicable for DS0, DS1, and DS3 transport.

4. Red alarms are used here only to illustrate the relationship with Yellow signals. Declaration of a Red alarm is an equipment issue and not specified by this standard.

10. Payload Pointers

10.1 STS-1 Payload Pointers

The STS-1 Payload Pointer provides a method of allowing flexible and dynamic alignment of the STS Synchronous Payload Envelope (SPE) within the STS Envelope Capacity, independent of the actual contents of the envelope.

Dynamic alignment means that the STS SPE is allowed to 'float' within the STS Envelope Capacity. Thus the pointer is able to accommodate differences not only in the phases of the STS SPE and the Transport Overhead, but in the frame rates as well.

10.1.1 Pointer Value

The payload pointer contained in H1 and H2 of the Line Overhead designates the location of the byte where the STS SPE begins. The 2 bytes allocated to the pointer function can be viewed as one word as shown in Figure 32. The last 10 bits (bits 7-16) of the pointer word carry the pointer value.

As illustrated in Figure 33, the pointer value is a binary number with a range of 0 to 782 which indicates the offset between the pointer and the first byte of the STS SPE. The Transport Overhead bytes are not counted in the offset such that a pointer value of 0 indicates that the STS SPE starts in the byte location that immediately follows the H3 byte (pointer action byte) whereas an offset of 87 indicates that the STS SPE starts immediately after the K2 byte.

10.1.2 Frequency Justification

If there is a frequency offset between the frame rate of the Transport Overhead and that of the STS SPE, then the pointer value will be incremented or decremented as needed, accompanied by a corresponding positive or negative stuff byte. Consecutive pointer operations must be separated by at least 3 frames in which the pointer value remains constant.

If the frame rate of the STS SPE is too slow with respect to that of the Transport Overhead, then the alignment of the envelope must periodically slip back in time and the pointer must be incremented by one. This operation is indicated by inverting bits 7,9,11,13, and 15 (I-bits) of the pointer word to allow 5-bit majority voting at the receiver. A positive stuff byte appears immediately after the H3 byte in the frame containing inverted I bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 34.

If the frame rate of the STS SPE is too fast with respect to that of the Transport Overhead, then the alignment of the envelope must be periodically advanced in time and the pointer must be decremented by one. This operation is indicated by inverting bits 8,10,12,14, and 16 (D-bits) of the pointer word to allow 5-bit majority voting at the receiver. A negative stuff byte appears in the H3 byte in the frame containing inverted D-bits. Subsequent pointers will contain the new offset. This is illustrated in Figure 35.

10.1.3 New Data Flag

Bits 1-4 (N-bits) of the pointer word carry a New Data flag. It is the mechanism which allows an arbitrary change of the value of the pointer if that change is due to a change in the payload.

Four bits are allocated to the flag to allow for error correction. The decoding may be performed by accepting NDF enabled if at least three bits match. Normal operation is indicated by a '0110' code in the N bits, NDF is indicated by inversion of the N bits to '1001'. The new alignment is indicated by the pointer value accompanying the New Data flag and takes effect at the offset indicated.

10.1.4 STS-1 Concatenation

A concatenation indication contained in the STS-1 payload pointer is used to show that the STS-1 is part of an STS-Nc.

The first STS-1 within an STS-Nc shall have a normal pointer word. All subsequent STS-1s within the group have their pointer values (bits 7-16) set to all '1's. Since this value does not indicate a valid offset, the pointer processors shall interpret this value to mean that they shall perform the same operations as performed on the first STS-1 within a STS-Nc. The New Data flag must be set when changing a pointer to/from the concatenation value.

10.1.5 Pointer Generation

The following list summarizes the rules for generating the STS-1 Pointer.

1. During normal operation, the pointer locates the start of the STS SPE within the STS Envelope Capacity. The New Data Flag is set to '0110'.
2. The pointer value can only be changed by operations 4, 5 or 6.
3. If an STS-Nc envelope is being transmitted, a pointer is generated for the first STS-1 only. The Concatenation Value is generated in place of the other pointers. All operations indicated by the pointer in the first STS-1 apply to each STS-1 in the STS-Nc.
4. If a positive stuff is required, the current pointer value is sent with the I-bits inverted and the subsequent positive stuff opportunity is filled with dummy information. Subsequent pointers contain the previous pointer value incremented by one. No subsequent increment or decrement operation is allowed for at least 3 frames following this operation.
5. If a negative stuff is required, the current pointer value is sent with the D-bits inverted and the subsequent negative stuff opportunity is overwritten with actual data. Subsequent pointers contain the previous pointer value decremented by one. No subsequent increment or decrement operation is allowed for at least 3 frames following this operation.
6. If the alignment of the envelope changes for any reason other than rules 4 or 5, the new pointer value shall be sent accompanied by the New Data Flag set to '1001.' The New Data Flag only appears in the first frame that contains the new value. The new envelope begins at the first occurrence of the offset indicated by the new pointer. No subsequent increment or decrement operation is allowed for at least 3 frames following this operation.

10.1.6 Pointer Interpretation

The following list summarizes the rules for interpreting the STS-1 Pointer.

1. During normal operation the pointer locates the start of the STS SPE within the STS Envelope Capacity.
2. Any variation from the current pointer value is ignored unless a consistent new value is received 3 times consecutively or it is preceded by one of rules 4, 5 or 6.
3. If the pointer value contains the Concatenation Value, then the operations performed on the STS-1 are identical to those performed on the first STS-1 within the STS-Nc. Operations 4 and 5 do not apply to this pointer value.
4. If the majority of the I-bits of the pointer word are inverted, a positive stuff operation is indicated. Subsequent pointer values shall be incremented by one.

5. If the majority of the D-bits of the pointer word are inverted, a negative stuff operation is indicated. Subsequent pointer values shall be decremented by one.
6. If the New Data Flag is set to '1001' then the coincident pointer value shall replace the current one at the offset indicated by the new pointer value regardless of the state of the receiver.

10.2 VT Payload Pointers

The VT Payload Pointer provides a method of allowing flexible and dynamic alignment of the VT SPE within the Virtual Tributary Superframe, independent of the actual contents of the envelope.

10.2.1 VT Pointer Value

The VT Payload Pointer word is shown in Figure 36.

The pointer value (bits 7-16) is a binary number which indicates the offset from V2 to the first byte of the VT SPE. The range of the offset is different for each of the VT sizes as illustrated in Figure 37. Note that the pointer bytes are not counted in the offset calculation.

10.2.2 VT Multiframe Indicator Byte (H4)

This byte indicates a variety of different superframes for use by certain sub-STS payloads. Specifically it provides:

- 500 microsecond (4 frame) superframe identifying frames containing VT pointers in the floating VT mode, and reserved byte locations in the locked VT mode.
- 2 ms (16 frame) superframe for Byte Synchronous out-slot-signaling for 2.048 Mbit/s payloads in the locked VT mode.
- 3 ms (24 frame) superframe for Byte Synchronous out-slot-signaling for DS1 payloads in the locked VT mode.

The value of the H4 byte read from the STS-1 SPE identifies the frame phase of the next STS-1 SPE. The coding of the H4 byte is illustrated in Figures 20, 38, 39, and 40.

For Network elements that operate only in the floating VT mode a simplified Multiframe Indicator byte may be used. The simplified version provides only the 500 microsecond superframe. The 2 or 3 ms superframe of any signaling within floating VTs is indicated by per-VT superframe indicators carried within the VT.

A converter from locked to floating VTs may pass Multiframe Indicator H4 through without any processing. However, a converter from floating to locked VTs must recover and align the superframes from all of the floating VTs and must generate the required Multiframe Indicator on the locked VT side.

10.2.3 VT Frequency Justification

The VT Payload Pointer is used to frequency justify the VT SPE in exactly the same way that the STS-1 Payload Pointer is used to frequency justify the STS SPE. A positive stuff opportunity immediately follows the V3 byte and V3 serves as the negative stuff opportunity such that when the opportunity is taken, V3 is overwritten by data. This is illustrated in Figure 37. The indication of whether or not a stuff opportunity has been taken is provided by the I - and D - bits of the pointer in the same VT superframe. The value contained in V3 when not being used for a negative stuff is not defined. The receiver is required to ignore the value contained in V3 whenever it is not used as a negative stuff.

10.2.4 VT Size

Bits 5 and 6 of the VT Payload Pointer indicate the size (x) of the VTx, and hence the VTx-1 SPE that the pointer is allowing to float. Four sizes are currently provided:

Size	Designation	VT Pointer Range (in 500 μsec)
00	VT6-1	0-427
01	VT3-1	0-211
10	VT2-1	0-139
11	VT1.5-1	0-103

Note that this technique for multiple sizes of Synchronous Payload Envelope is only used at the VT level at this time.

10.2.5 New Data Flag

Bits 1-4 (N-bits) of the pointer word carry a New Data Flag. It is the mechanism which allows an arbitrary change of the value of a pointer, and possibly also the size of the VT, if that change is due to a change in the payload. If the change includes a change in size then, implicitly, there must be a simultaneous new data transition in all of the VTs in the VT Group.

As with the STS-1 Pointer New Data Flag, the normal value is '0110' (transmitted), and the value '1001' (received exactly) indicates a new alignment for the envelope, and possibly new size. If a new size is indicated, then all VT pointers (1 to 4), in the VT Group must simultaneously indicate NDF with the same new size. The new alignment, and possibly size, is indicated by the pointer value and size value accompanying the New Data Flag and takes effect at the offset indicated.

10.2.6 VT Concatenation

Sub-STS-1 services which require N times VTx-1 rates can be transported by concatenated VTx-Nc's whose constituent VTx-1s are kept together in a way to assure phase and sequence integrity.

As with the STS-1 Payload Pointer, the VT Payload Pointer uses the Concatenation Value (all '1's in bits 7-16) to indicate that the VTx-1s are concatenated. This function is only defined for VT6-1s to form VT6-Nc's at this time. If a pointer contains the Concatenation Value, it is an indication to the pointer processor that this VTx-1 is concatenated to the previous VTx-1, and all operations indicated by the previous pointer are to be performed on this VTx-1 as well. (Mechanisms for concatenation of non-contiguous VTx-1s are for further study.)

10.2.7 VT Pointer Generation and Interpretation

The rules for generating and interpreting the VT Payload Pointer for the VT SPE are an extension to the rules provided in Sections 10.1.5 and 10.1.6 for the STS-1 Payload Pointer with the following modifications:

1. The term STS SPE is replaced with VT SPE.
2. Additional Pointer Generation Rule 7: If the size of the VTs within a VT Group is to change, then a New Data Flag, as described in rule 6, is to be sent in all VTs of the new size in the group simultaneously.

3. Additional Pointer Interpretation Rule 7: If a New Data Flag of '1001' and an arbitrary new size of VT are received simultaneously in all of the VTs within a VT Group, then the coincident pointers and sizes shall replace the current ones immediately.

11. Multiplex Procedure

11.1 Byte Interleaved Multiplexing

The STS-1 input signals shall be interleaved byte-wise to form the STS-N signal. The first byte of the STS-N signal shall be the A1 framing byte from STS-1 #1 followed sequentially by the A1 byte from STS-1 #2 through #N. The first bit to be transmitted shall be the most significant bit of the A1 framing byte from STS-1 #1.

Before byte interleaving STS-1 signals to form STS-N signal all of the transport overhead in the signals to be interleaved must be frame aligned. The alignment is accomplished by adjusting the pointer values of the STS-1s to reflect the new relative positions of the STS Synchronous Payload Envelopes (SPEs).

11.2 STS-N Interleaving

If an STS-M level signal is input to a byte interleaver with STS-N level output, M bytes of STS-M are consecutively placed on the output STS-N signal. This method of interleaving is illustrated in Figure 41 where STS-X, STS-Y and STS-Z (X+Y+Z=N) inputs are sequentially interleaved to form an STS-N output.

11.3 Scrambling

A frame synchronous scrambler of sequence length 127, operating at the line rate, shall be used. The generating polynomial shall be $1+x^6+x^7$.

The scrambler shall be reset to '11111111' on the most significant bit (see Figure 3) of the byte following the STS-1 #N C1 (STS-1 ID) byte. This bit, and all subsequent bits to be scrambled shall be added, modulo 2 to the output from the x^7 position of the scrambler, as shown in Figure 42. The scrambler shall run continuously throughout the complete STS-N frame.

The frame bytes A1 and A2 and the STS-1 identification byte C1 from STS-1 #1 through STS-1 #N shall not be scrambled.

11.4 STS-1 Frame and OC-N Line Signal Composition

The flow chart shown in Figure 43 illustrates the stages in the formation of an STS-N level signal and is described in the following. Initially, the content of an STS-1 SPE is formed from VTs or a bulk mapped DS3 for example. Included within the STS-1 SPE are the nine bytes comprising the STS Path Overhead. Of these, the BIP-8 error check byte (B3) is calculated over the entire contents of the STS-1 SPE and the result is placed in the B3 byte of the following frame.

For super rate payloads, the STS-1 Concatenation Process (described in section 10.1.4) results in the STS POH always appearing in the first STS-1 of the STS-Nc signal. Furthermore, in this case, the B3 BIP-8 error check byte is calculated over the entire STS-Nc SPE on a frame by frame basis, and the result is again placed in B3 of the following frame.

In the event that the contents of the STS SPE are lost, due for example to the failure of an OC-N signal input to an OC-N/M multiplex, then an all '1's condition is substituted. This is the STS Path AIS condition referred to in Figure 43.

At this point in the multiplex process, an STS SPE Unequipped is indicated by substituting an all '0's pattern.

The next stage involves the addition of the Line Overhead. Of this overhead only B2, H1, H2, H3, Z1 and Z2 are present on a per STS-1 basis in an STS-N signal. Thus, Line level BIP-8 Error checking and STS-1 payload pointer processing are actually performed on each individual STS-1 irrespective of the presence of concatenated STS-1s.

The remaining bytes of the Line Overhead (APS K1 and K2, Data Com D4–D12 and Orderwire E2) are limited to the first STS-1 in any STS-N signal. The content of the unused bytes within STS-1 #2 through to STS-1 #N is not specified.

A failure at the input to an OC-N line repeater will result in the substitution of Line AIS at this point.

The final part of the overhead, the Section Overhead is added next. As with the Line Overhead, it is important to note that not all of these bytes occur on a per STS-1 basis. The Section BIP-8 (B1), Orderwire (E1), User Channel (F1) and Data Com channel (D1-D3) are present only in STS-1 #1 of any STS-N signal.

The complete STS-1 signals are now ready for byte interleave multiplexing to the STS-N level as described in Section 11. The STS-N signal is then serialized after which it is scrambled with the exception of all N A1, A2 and C1 bytes. The final operation is the calculation of the Section level BIP-8 (B1) byte over the entire STS-N bit stream on a frame by frame basis (i.e. N times 6480 bits). The result is loaded into the B1 byte of STS-1 #1 in the following frame at the point where Section Overhead is inserted.

12. Payload Mapping

This section discusses the mapping of network services into STS SPEs. This includes STS-1 level services, sub-STS-1 level services, and super-rate STS-Nc services.

12.1 Sub-STS-1 Level Mappings

This section describes the payload mappings that use the VT-structured STS-1.

12.1.1 DS1 Payload Mappings

All DS1 Payloads are mapped into the VT1.5 SPE.

12.1.1.1 Asynchronous Mapping for DS1

The asynchronous mapping for DS1 is depicted in two representations in Figures 44 and 45.

In addition to the VT Path Overhead, the DS1 mapping consists of 771 data bits, 6 stuff control bits, 2 stuff opportunity bits, and 8 overhead communication channel bits. The remaining bits are Fixed Stuff (R) bits. The 8 O-bits are reserved for future communication purposes.

Two sets (C1, C2) of 3 stuff control bits are used to control the 2 stuff opportunities, S1 and S2 respectively. C1 C1 C1 = 0 0 0 indicates that S1 is a data bit while C1 C1 C1 = 1 1 1 indicates that S1 is a stuff bit. C2 controls S2 in the same way. Majority vote should be used to make the stuff decision in the desynchronizer for protection against single bit errors in the C bits.

The stuffing mechanism which generates the C-bits must be chosen such that given a desynchronizer with 175 Hz 3 dB bandwidth 2nd order Low Pass (LP) filter, the output jitter shall be less than 1.0 Unit Interval (UI) Peak-to-Peak and 0.3 UI RMS assuming no input jitter at the synchronizer.

The value contained in S1 and S2 when they are stuff bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as stuff bits.

12.1.1.2 Bit Synchronous Mapping for DS1

The bit synchronous mapping for DS1 is depicted in Figure 46.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous DS1.

12.1.1.3 Byte Synchronous Mapping for DS1

The byte synchronous mapping for DS1 is depicted in Figure 47.

The S1, S2, S3, and S4 bits contain the signaling for the 24 DS0 channels. The phase of the signaling bits is indicated in the P1 and P0 bits in Floating VT Mode, and in the Multiframe Indicator byte (H4) in Locked VT Mode. This is illustrated in Figure 48.

12.1.2 Asynchronous Mapping for DS1C

The asynchronous mapping for DS1C is mapped into a VT3 as illustrated in Figure 50.

In addition to the VT Path Overhead, the DS1C mapping consists of 1574 data bits, 12 stuff control bits, 4 stuff opportunity bits, and 16 overhead communication channel bits. The remaining bits are Fixed Stuff (R). The O bits are reserved for future overhead communication purposes.

Two sets (C1, C2) of 3 stuff control bits are used to control the 2 stuff opportunities S1 and S2 respectively. C1 C1 C1 = 0 0 0 indicates that S1 is a data bit while C1 C1 C1 = 1 1 1 indicates that S1 is a stuff bit. C2 controls S2 in the same way. Majority vote should be used to make the stuff decision in the desynchronizer for protection against single bit errors in the C bits.

The stuffing mechanism which generates the C-bits must be chosen such that given a desynchronizer with 350 Hz 3 dB bandwidth 2nd order LP filter, the output jitter shall be less than 1.0 UI Peak-to-Peak and 0.3 UI RMS assuming no input jitter at the synchronizer.

The value contained in S1 and S2 when they are stuff bits is not defined. The receiver is required to ignore the value in these bits whenever they are used as stuff bits.

12.1.3 Asynchronous Mapping for DS2

The asynchronous DS2 is mapped into a VT6 as illustrated in Figure 51.

In addition to the VT Path Overhead, the DS2 mapping consists of 3152 data bits, 24 stuff control bits, 8 stuff opportunity bits, and 32 overhead communication channel bits. The remaining bits are Fixed Stuff (R). The O bits are reserved for future overhead communication purposes.

Two sets (C1, C2) of 3 stuff control bits are used to control the 2 stuff opportunities S1 and S2 respectively. C1 C1 C1 = 0 0 0 indicates that S1 is a data bit while C1 C1 C1 = 1 1 1 indicates that S1 is a stuff bit. C2 controls S2 in the same way. Majority vote should be used to make the stuff decision in the desynchronizer for protection against single bit errors in the C bits.

The stuffing mechanism which generates the C-bits must be chosen such that given a desynchronizer with 500 Hz 3 dB bandwidth 2nd order LP filter, the output jitter shall be less than 1.0 UI Peak-to-Peak and 0.3 UI RMS assuming no input jitter at the synchronizer.

The value contained in S1 and S2 when they are stuff bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as stuff bits.

12.1.4 2.048 Mbit/s Payload Mappings

All 2.048 Mbit/s payloads are mapped into the VT2 SPE.

Note: The 2.048 Mbit/s mappings provided in this standard are provisional and subject to further study. It is the intention to review similar mappings proposed in CCITT and in those countries where 2.048 Mbit/s hierarchies are predominant and consider modifications of the 2.048 Mbit/s mappings presented here so as to foster compatibility and interworking to the greatest extent. At the present time, an electrical interface for 2.048 Mbit/s has not been standardized by ANSI/T1.

12.1.4.1 Asynchronous Mapping for 2.048 Mbit/s

A tentative asynchronous 2.048 Mbit/s mapping is depicted in two representations in Figures 52 and 53.

In addition to the VT Path Overhead, the mapping consists of 1023 data bits, 6 stuff control bits, 2 stuff opportunity bits, and 8 overhead communication channel bits. The remaining bits are Fixed Stuff (R) bits. The O bits are reserved for future overhead communication purposes.

Two sets (C1, C2) of 3 stuff control bits are used to control the 2 stuff opportunities S1 and S2 respectively. C1 C1 C1 = 0 0 0 indicates that S1 is a data bit while C1 C1 C1 = 1 1 1 indicates that S1 is a stuff bit. C2 controls S2 in the same way. Majority vote should be used to make the stuff decision in the desynchronizer for protection against single bit errors in the C bits.

The stuffing mechanism which generates the C-bits must be chosen such that given a desynchronizer with 300 Hz 3 dB bandwidth 2nd order LP filter, the output jitter shall be less than 1.0 UI Peak-to-Peak and 0.3 UI RMS assuming no input jitter at the synchronizer.

The value contained in S1 and S2 when they are stuff bits is not defined. The receiver is required to ignore the value contained in these bits whenever they are used as stuff bits.

12.1.4.2 Bit Synchronous Mapping for 2.048 Mbit/s

A tentative bit synchronous mapping for 2.048 Mbit/s is depicted in Figure 54.

Note that a common desynchronizer can be used for both asynchronous and bit synchronous 2.048 Mbit/s.

12.1.4.3 Byte Synchronous Mapping for 2.048 Mbit/s

Figure 55 shows a tentative byte synchronous mapping for 30 channel, 2.048 Mbit/s tributaries employing Channel Associated Signaling (CAS). Signaling is carried in byte 19. The signaling assignments are shown in Figure 49.

A tentative byte synchronous mapping for 31 channel tributaries is shown in Figure 56. Byte 19 carries tributary channel 16.

The S1, S2, S3, and S4 bits contain the signaling for the 30 DS0 channels. The phase of the signaling bits is indicated in the PI and P0 bits in Floating VT mode, and in the Multiframe Indicator byte (H4) in Locked VT mode. This is illustrated in Figure 49.

12.2 STS-1 Level Mappings

This section describes mappings that occupy an entire STS-1 SPE.

12.2.1 Asynchronous Mapping for DS3

The asynchronous mapping for DS3 is mapped into an STS-1 SPE as shown in Figure 57.

The mapping consists of 9 subframes every 125 microseconds. Each subframe consists of 621 data bits, a set of 5 stuff control bits, 1 stuff opportunity bit, and 2 overhead communication channel bits. The remaining bits are Fixed Stuff (R) bits. The O bits are reserved for future overhead communication purposes.

The set of 5 stuff control bits (C1-5) is used to control the stuff opportunity (S) bit. C C C C C = 0 0 0 0 0 indicates that the S bit is a data bit, whereas C C C C C = 1 1 1 1 1 indicates that the S bit is a stuff bit. Majority vote should be used to make the stuff decision in the desynchronizer for protection against single and double bit errors in the C bits.

The value contained in the S bit when not used is not defined. The receiver is required to ignore the value contained in this bit whenever it is used as a stuff bit.

12.2.2 Byte Observable SYNTRAN Mapping

SYNTRAN (see Reference [4]) specific overhead (framing, CRC-9, and triad numbering) is discarded or created at the STS-1 interface. SYNTRAN Local and End-to-End Embedded Operations Channels (EOCs) are terminated at the STS-1 interface. The 64 kbit/s Facility Data Link is normally terminated and combined with the Line Layer Data Com channels. Optionally, it can be transported in the Path Layer User Channel (F2). Figure 58 shows the mapping of the SYNTRAN payload into the STS-1 SPE. The 672 Main Information Time Slots, bytes B1 through B672, are sequentially mapped starting at Row 2, Column 2, ending with Row 9, Column 87, and skipping Columns 1, 30, and 59. The F bit and signaling information in B673 through B690 is placed in Row 1, Columns 60 through 87. This information is distributed on a per column basis as shown in Figure 59D. B691, and the LLDL (Low Level Data Link) are placed in Column 30, Rows 2 and 3, respectively. An additional Auxiliary Byte is defined in Row 1 of this column to transport B676, b4-b7 and for B691 and LLDL data present flags. The assignments for this additional SYNTRAN information are shown in Figures 59A, 59B, and 59C. The SYNTRAN Signaling Phase Indicator (B676, b4 and b5) and the signaling information must be aligned with the Multiframe Indicator Byte (H4), P1 and P0 bits.

Note that this mapping is end-to-end compatible with 28 Locked mode VT1.5s carrying bit or byte synchronous DS1s with the exception of the B676, B691 and LLDL bytes.

12.3 Super-rate Mappings

For further study.

13. Automatic Protection Switching

13.1 Protection Switching Boundaries

This standard only addresses protection of the optical line. All signals (N x STS-1) are switched simultaneously. Protection covers the multiplexer/optics units from the point where the Line Overhead is inserted (the head end), to the point where it is terminated (the tail end).

13.1.1 1+1 Protection Switch

A 1+1 Protection Switch architecture used for optical protection switching is defined as follows:

> An architecture where the head end optical signal is bridged to working and protection equipment such that the same optical signal is transmitted identically to the tail end working and protection equipment. On the tail end, each working and protection optical signal is monitored independently and the same way for failures. The receive equipment selects either the working or protection optical signal as the one carrying service based on switch initiation criteria outlined in Section 13.2.

The default operation switch shall be unidirectional switching. The default operation may be overridden by local commands or over the data communications channel.

The 1+1 architecture may be made revertive or non-revertive. A 1+1 node, as an option, may be upgradable to 1:n.

Note for 1+1 architectures provisioned as unidirectional at both ends, the APS channel (bytes K1 and K2) must still be used for indicating manual operation. Further, bit 5 of byte K2 shall be set to '0' (see Section 13.5.2.1). If either the transmitted or received bit 5 of byte K2 indicates 1+1 protection switching, then the corresponding optical line shall be protected using 1+1 protection switching as described in this section.

13.1.2 1:n Protection Switch

A 1:n Protection Switch architecture is defined as follows:

> An architecture where any one of n optical working channels can be bridged to a single optical protection channel. Permissible values of n are from 1 to 14. Head end to tail end communications are accomplished by using the APS channel (bytes K1 and K2). All switching must be revertive.

The default operation shall provide bidirectional switching. If both ends of the system are optioned for uni-directional switching, then uni-directional switching shall be provided. The default operation may be overridden by local commands or over the data communications channel.

For 1:n architectures where n=1, the local protection switch controller must be capable of placing itself in a provisioned state that is compatible with the 1+1 architecture previously described to allow interworking between the two architectures.

13.2 Switch Initiation Criteria

Two automatic protection switch initiation criteria shall be provided:

Signal Fail (SF)	"Hard" failure caused by loss of OC-N frame within an optical signal, or by some detectable hard failure (e.g., stuck bit) or a BER exceeding a specified value.
Signal Degrade (SD)	"Soft" failure caused by a BER exceeding a pre-selected threshold. A composite measure obtained by summing the parity violations detected in each STS-1 Line BIP-8 (Byte B2) of an OC-N is used to monitor the complete optical channel. The specific BER used to define the threshold is an equipment issue but is typically in the range 10^{-6} to 10^{-9}.

A hold-off time is typically allowed in order to verify detection of these conditions prior to switch initiation.

13.2.1 Wait to Restore

To prevent potential "chattering" of the protection switch due to an intermittent failure, the working channel must be fault free for a fixed period of time before the switch is taken down. This period is called Wait to Restore (WTR). The duration of the Wait to Restore period is an equipment specification and is typically 5 minutes. A signal failure or signal degrade on another channel overrides the Wait to Restore.

13.3 Switch Commands

The following protection switch commands shall be provided:

Forced Switch	Transfers the working channel to protection regardless of the state of the protection channel.
Manual Switch	Transfers the working channel to protection only if the protection channel is working fault free and if the protection channel is not carrying higher priority traffic.

13.4 Switch Request Priorities

The following lists all switch actions in descending order of priority.

- Lockout
- Forced Switch
- Automatic Switch - Signal Fail
- Automatic Switch - Signal Degrade
- Manual Switch
- Wait to Restore

In the event of equal priority switch requests the following rules shall apply:

- A high priority channel shall preempt a low priority channel
- If channel priority is equal, then the first failure or command shall have priority
- If requests of equal priority occur simultaneously, then the lowest channel number takes priority.

13.5 APS Byte Definition

Two bytes are used as defined in the following sections. See also Section 13.6 for details on operational usage of these bytes.

13.5.1 Byte K1

13.5.1.1 Bits 1-4 Switch Priority

Switch priority is a combination of switch request priority (bits 1-3) and working channel priority (bit 4) as indicated in the table below.

Bit 1234	Condition
1111	Forced Switch - High Priority
1110	Forced Switch - Low Priority
1101	Signal Fail - High Priority
1100	Signal Fail - Low Priority
1011	Signal Degrade - High Priority
1010	Signal Degrade - Low Priority
1001	Manual Switch - High Priority
1000	Manual Switch - Low Priority
0111	Wait to Restore - High Priority
0110	Wait to Restore - Low Priority
0101	Exerciser - High Priority
0100	Exerciser - Low Priority
0011	Reverse Request (bi-directional switch) - High Priority
0010	Reverse Request (bi-directional switch) - Low Priority
0001	No bridge required - High Priority (Not Used)
0000	No bridge required - Low Priority

Note 1: Lockout is not included in this table because lockout can be implemented at the receive end in isolation. There is no need to specifically signal the existence of a lockout condition to the head end.

Note 2: For all cases in this table, bit 4 indicates the priority assigned to the working channel for which the switch action is being requested.

13.5.1.2 Bits 5-8 Bridge Order Channel Number

1-14	Working channel number
0	No bridge required, the protection channel is supplied with a signal containing valid Transport Overhead for carriage of the APS bytes and Line BIP-8.
15	Extra Traffic, the protection channel must be bridged to the extra traffic input.

When channel #0 is selected, the condition bits (bits 1-4, byte K1) shall show the received protection channel status (e.g., no bridge required, signal degrade, etc.). When channel #15 is selected, the condition bits shall show the priority to be assigned for bridging extra traffic.

13.5.2 Byte K2

13.5.2.1 Bit Assignments

Bits 1-4	Channel number of the traffic being carried.
Bit 5	1 = 1:n protection switching 0 = 1+1 protection switching
Bits 6-8	Reserved for future use for drop and insert protection (nested switching). Note that code '111' and '110' will not be used in order to avoid false Line AIS and Line FERF indications.

Byte K1 and bits 1-5 of byte K2 shall be transmitted on the protection channel and may also be transmitted on working channels.[5] The defined codes for Line FERF and Line AIS must be transmitted via byte K2 on each working channel, when appropriate.

Before accepting the APS byte as valid, the message must be received identically in three successive frames.

13.5.2.2 Line AIS and Line FERF

Notice that byte K2 is also used to indicate Line AIS or Line FERF on all channels, including the protection channel (see Section 9.4.1). The coding of byte K2 described in the previous section, including bits 6-8 which have not been specified in detail at this time, does not and will not include this all '1's code or code '110' in bits 6-8.

5. Receivers cannot assume that the K1 byte will be transmitted on working channels.

13.6 Switch Operation

13.6.1 1:n Bi-Directional Switching

When a fail condition is detected or a switch command is received at the tail (receive) end of a system, the protection logic compares the priority of this new condition with the priority of the channel (if any) using protection. This includes the priority of any bridge order. If the new request is higher priority, then APS byte K1 is loaded with the condition and the number of the channel requesting use of the protection channel. At the head (transmit) end site when the new APS byte K1 has been verified the channel is bridged to protection, APS Byte K2 is set to show the channel number of the traffic on the protection channel. Byte K1 is set to order a bridge for that channel with reverse request condition. This initiates the bi-directional switch. Appendix B illustrates the protection switching action for a 1:n bi-directional switching example.

At the tail end the switch to protection is completed when, the channel # in APS byte K2 matches the number of the channel requesting the switch and the fault condition (if any) on the protection channel in either direction is less severe than the condition on the working channel. The tail end will also bridge as ordered by APS byte K1 and the head end will complete the bi-directional switch when it receives the proper K2.

When the switch is no longer required, i.e. system has been repaired and wait to restore has expired or the switch command is released, the tail end releases the switch and sets the channel number in APS byte K1 (bits 5-8) to '0000' and condition (bits 1-4) to '0000'.

The head end then releases the bridge and switch. The APS byte K1 channel number is also set to '0000' this causes the tail end to release the bridge.

When protection channel is not in use, it must be provided with a signal containing valid Transport Overhead for carriage of the APS bytes and Line BIP-8. This may be achieved by bridging it to a working channel. The choice of which working channel is bridged, is not covered by this specification, and can be made by the transmit end. Any channel is valid, and the receive end must not assume or require any specific channel.

The APS byte K2 channel number must always indicate the channel number of the traffic being carried. If the signal is not one of the working channels, or extra traffic, (e.g., a test signal) channel #0000 shall be used.

13.6.2 1:n Uni-Directional Switching

All actions are as described in Section 13.6.1 except that the usage of the reverse direction of the protection channel and the incoming bridge orders are not considered and the bridge orders are not issued for the reverse direction of traffic.

13.6.3 1+1 Switching

When a fault is detected or a switch request is received the tail (receive) end evaluates the conditions as above and can switch immediately since the head end is already bridged. For bi-directional switching, APS byte K1 is used as above to complete the switch at the other end of the system.

14. Data Communications Channels

14.1 Line and Section Data Communications Channel Usage

The optical interface specified contains two data communications channels to be used as embedded operations channels to communicate to each Network Element. These channels shall not be used as individual 64 kbit/s channels but as a single portion of bandwidth (192 kbit/s in the case of the Section Data Communications Channel and 576 kbit/s in the case of the Line Data Communications Channel). Further the protocol for these channels is packet oriented. Figure 60 illustrates some of the configurations that can result during the process of building a network with standard optical transmission equipment. In Figure 60, a hub is illustrated by three interconnected LTEs. The interconnection provides a logical relay function to allow packets to be transferred from one LTE to another. The following sections refer to Figure 60 to explain how each of the data communications channels is used.

14.1.1 Section Data Communications Channel

The Section Data Communications Channel is used for applications of Operations, Administration, Maintenance and Provisioning in the network. Since all Network Element types (Section, Line or Path Terminating Equipment) have some physical embodiment, and hence physical maintenance needs, it follows that all Network Elements must support the Section Data Link. Its function is to communicate messages between Network Elements connected in a point to point manner. Point-to-point links can be connected at the regenerators by using a logical relay function. Therefore, as Figure 60 shows, it is used for communication between LTEs, repeaters and add/drop multiplexers.

Multiple sections (links between Section Elements), bounded by Line Termination Equipment, form a domain of interest called a "Section Domain."

The Section Data Communications Channel is used for communication between Section Elements within a Section Domain. The Logical Line channel is used to communicate to Section Domains as single entities, or via a gateway function to Section Elements within that Section Domain.

14.1.2 Logical Line Channel

The Logical Line Channel can be transported on the Line Data Communications Channel or on a logical channel established in the Section Data Communications Channel in applications where physically terminating the Line Data Communications Channel is not justified (e.g., in small networks or sub-networks).

14.2 Data Communications Channel Protocols

14.2.1 Section Data Communications Channel Protocols

The following table specifies the protocol stack for the first three layers of the Section Data Communications channel:

Layer 1	Section Data Communications Channel (Bytes D1, D2 and D3)
Layer 2	LAPD
Layer 3	ISO 8473

Values for many parameters for each of these protocols must still be specified to ensure interoperability. Examples of such parameters are maximum information field size, maximum number of outstanding I-frames, levels of priority, timers and values of SAPI and TEI fields.

These parameters are for further study.[6] The SAPI values currently reserved by CCITT Recommendation Q.921 (i.e., 0, 1, 16, 63, and 127) will not be used other than in ways consistent with Q.921.

14.2.2 Line Data Communications Channel Protocols

For further study.

6. Discussion of these currently focuses on the following values: maximum information field (LAPD), 1024 bytes; maximum number of outstanding I-frames (LAPD), 7 or 127; and levels of priority (ISO 8473), ≤ 7.

TABLE 1 - STANDARD OC RATES	
OC LEVEL	LINE RATE (Mbit/s)
OC-1	51.840
OC-3	155.520
OC-9	466.560
OC-12	622.080
OC-18	933.120
OC-24	1244.160
OC-36	1866.240
OC-48	2488.320

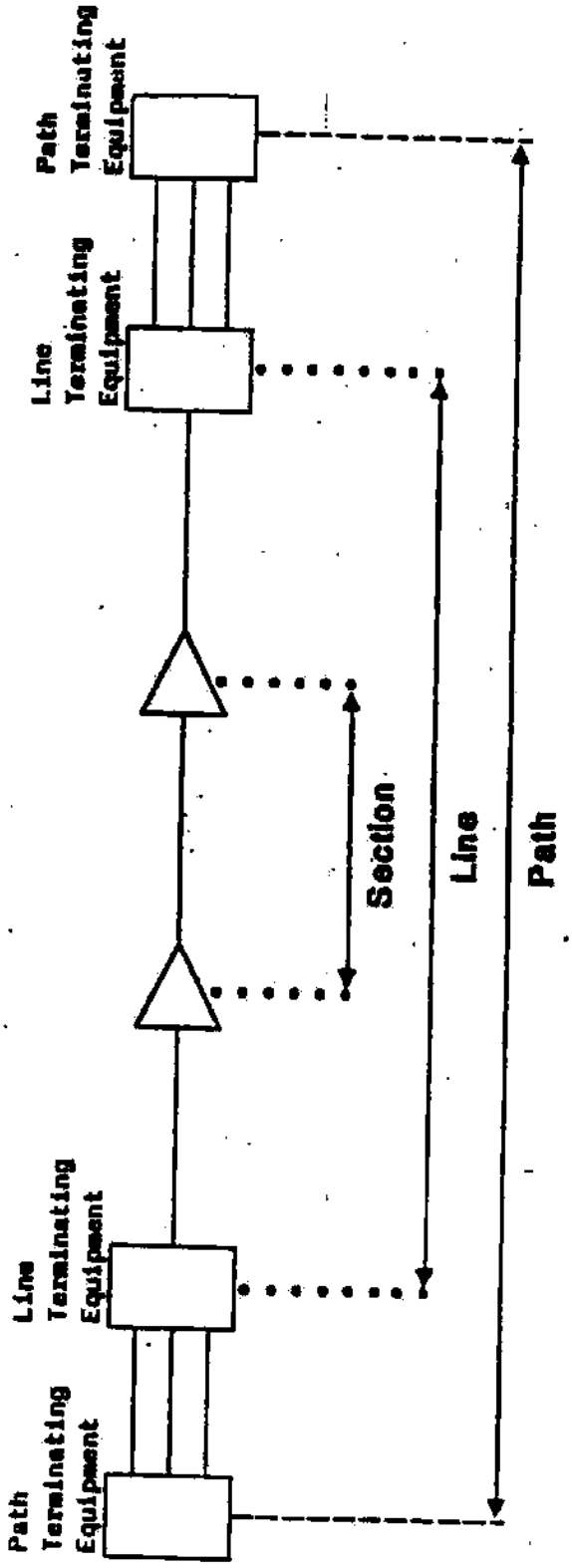


FIGURE 1 – SIMPLIFIED DIAGRAM DEPICTING LINE, PATH, AND SECTION DEFINITIONS

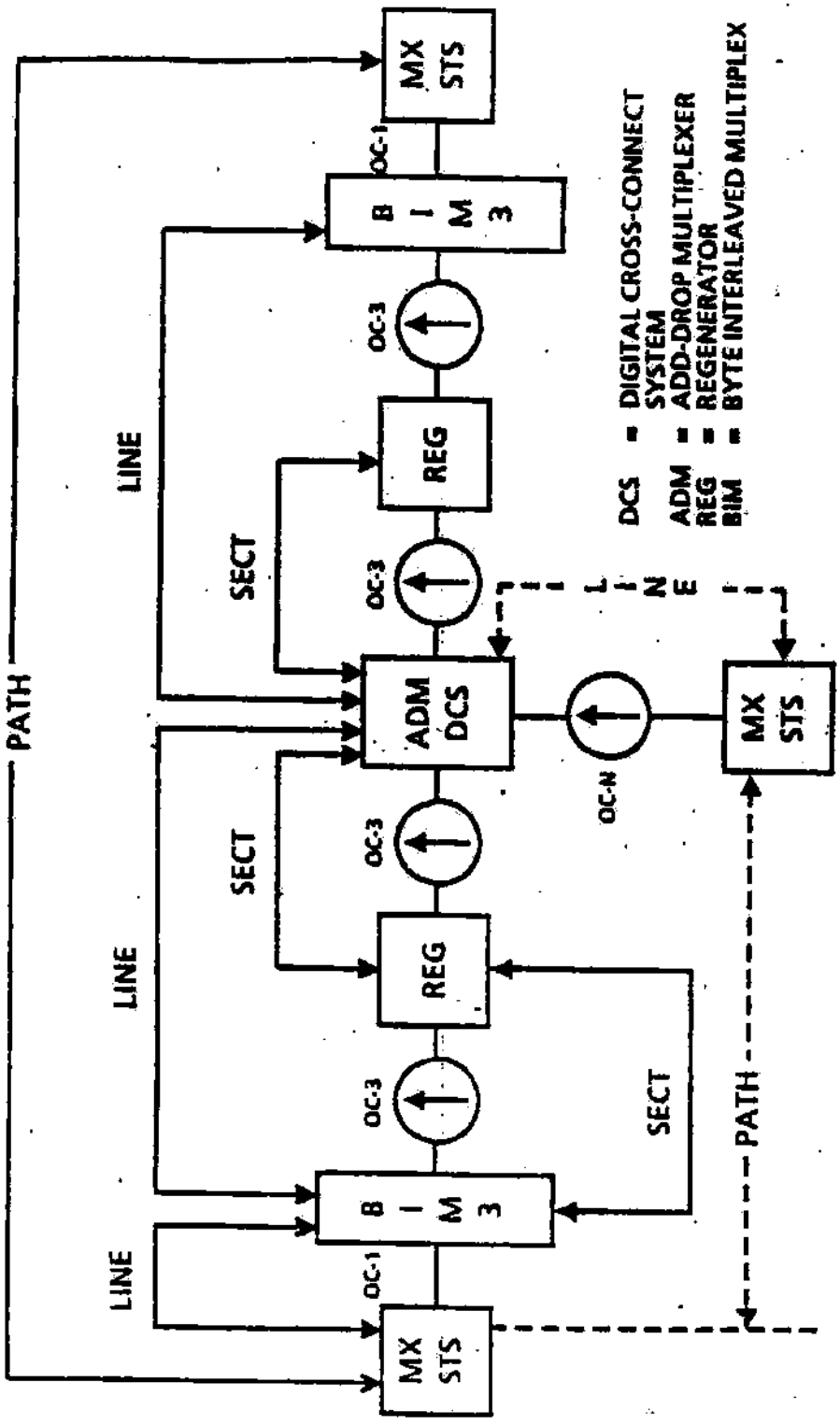


FIGURE 2 - DIAGRAM ILLUSTRATING LINE, PATH AND SECTION DEFINITIONS

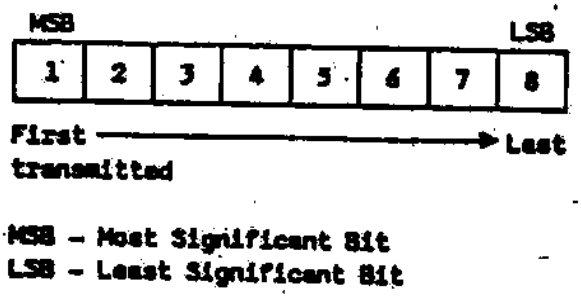
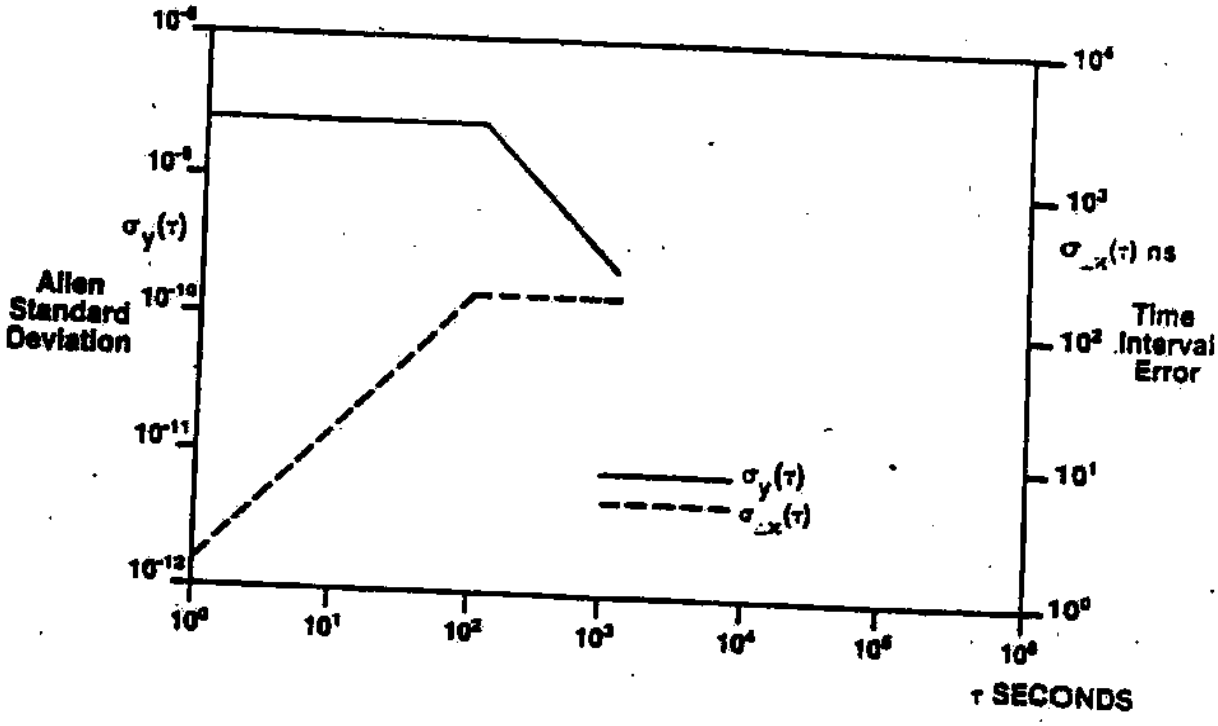


Figure 3 – Bit Position Numbering



Input Timing Signal 1 μsec p-p Bandlimited Whitenoise

Bandwidth 150Hz

FIGURE – 4 PROVISIONAL CLOCK SHORT TERM STABILITY REQUIREMENTS

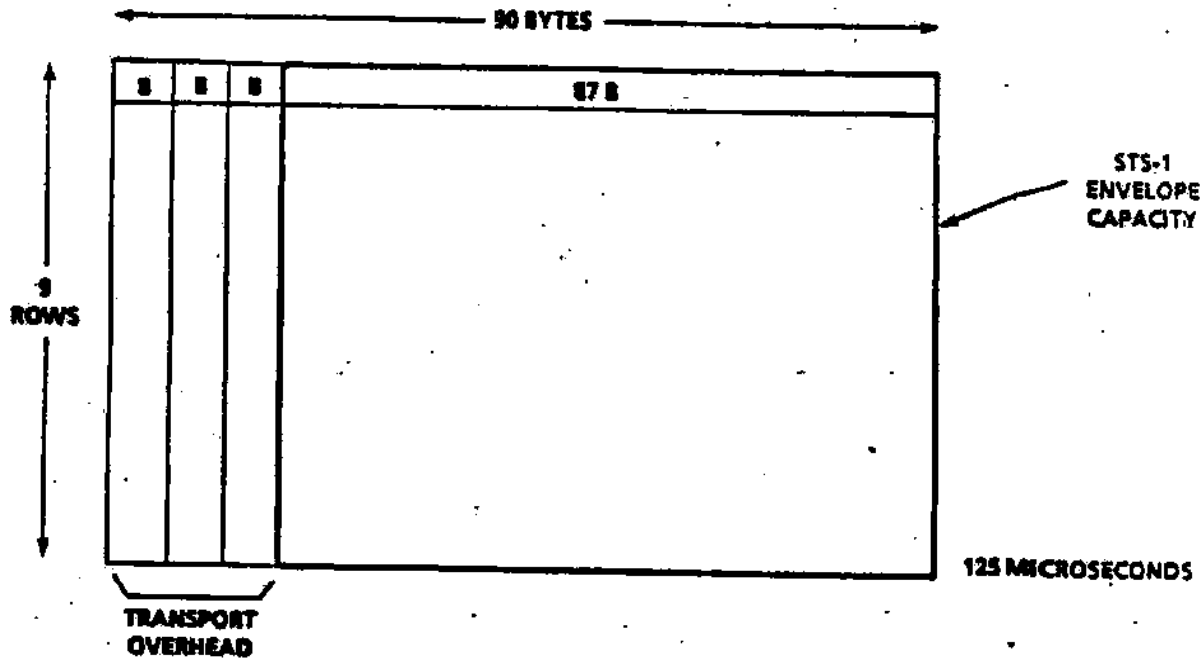


FIGURE 5 - STS-1 Frame

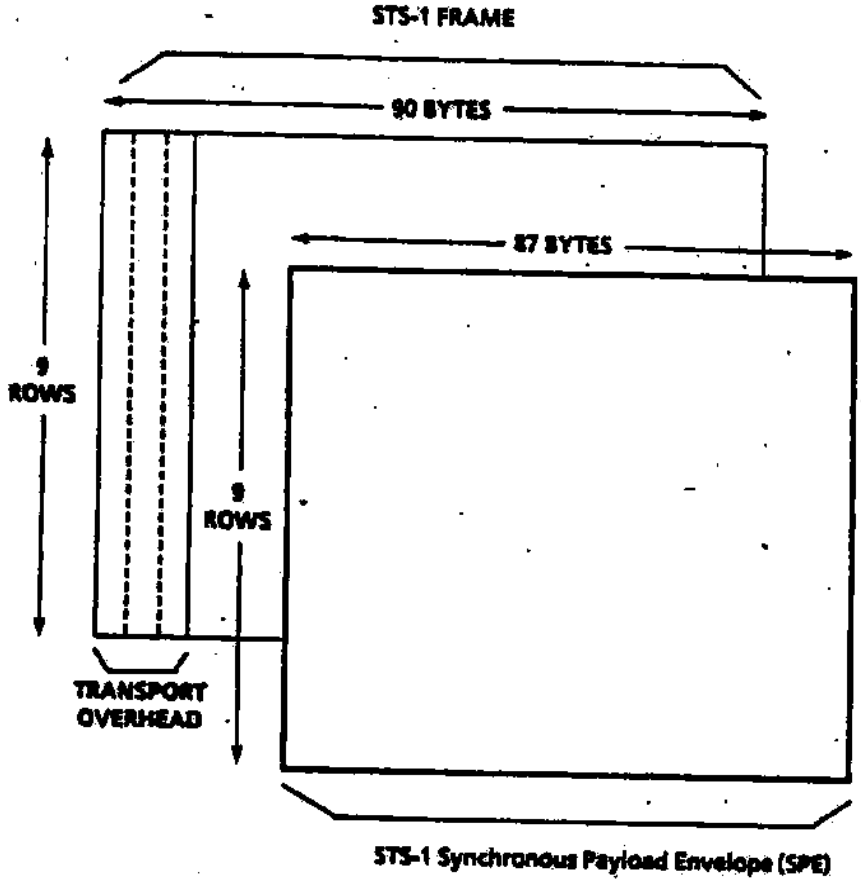


FIGURE 6 - SYNCHRONOUS PAYLOAD ENVELOPE (SPE)

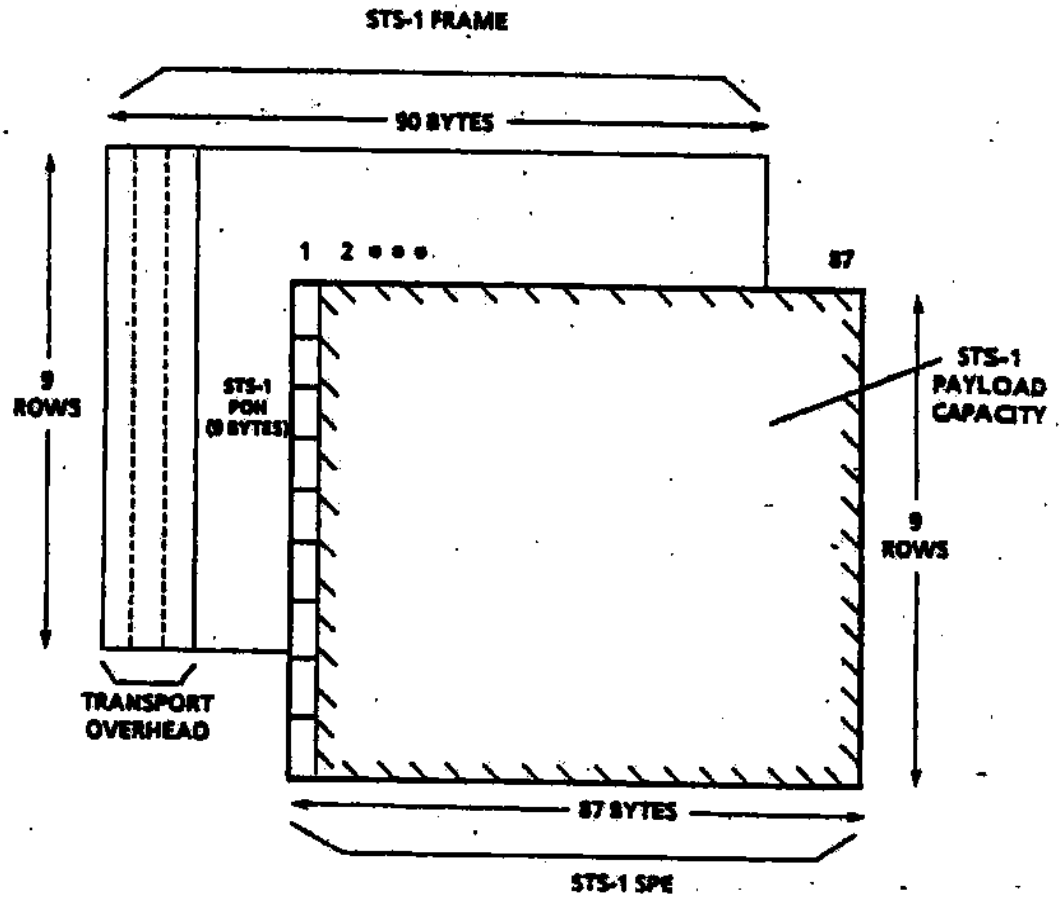


FIGURE 7 - STS-1 SYNCHRONOUS PAYLOAD ENVELOPE WITH STS-1 POH AND STS-1 PAYLOAD CAPACITY ILLUSTRATED

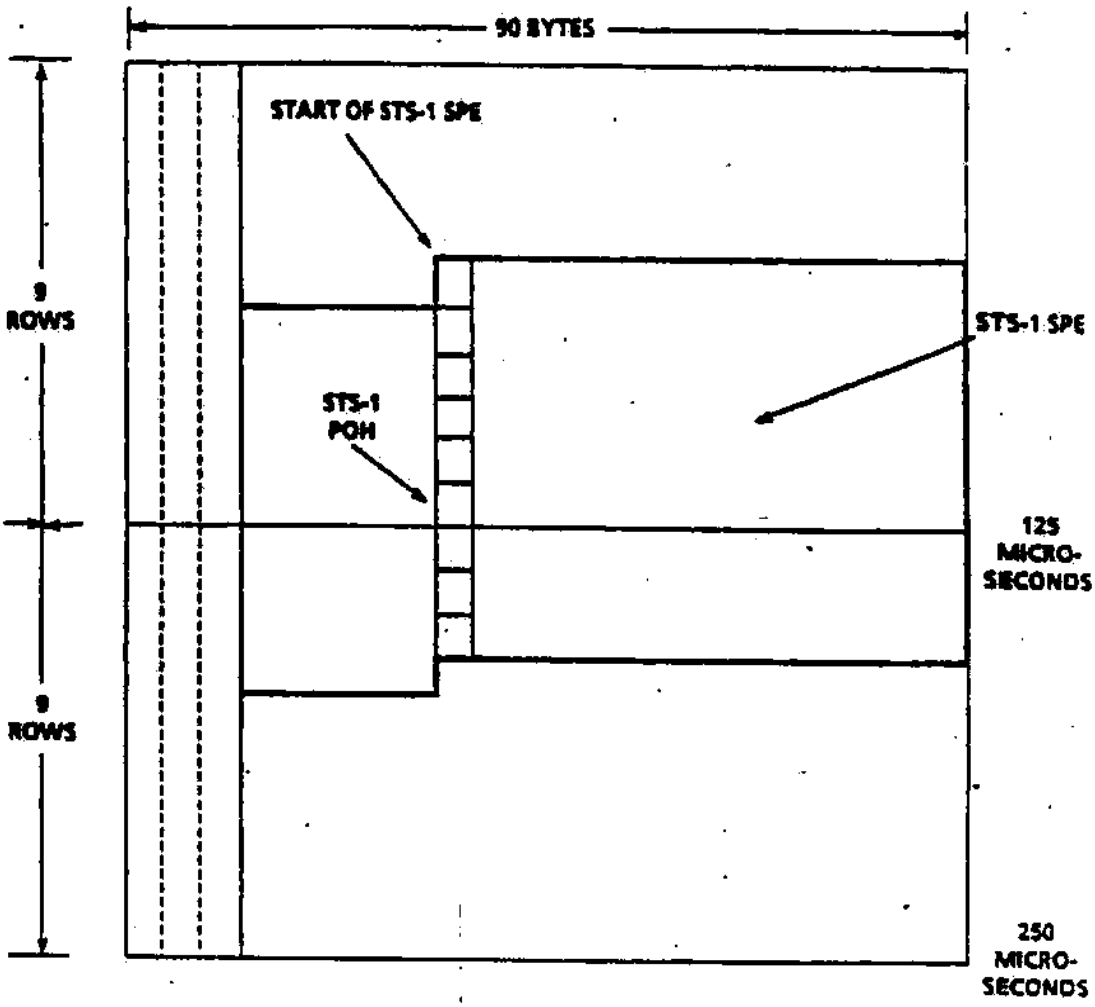


FIGURE 8 - STS-1 SPE IN INTERIOR OF STS-1 FRAME

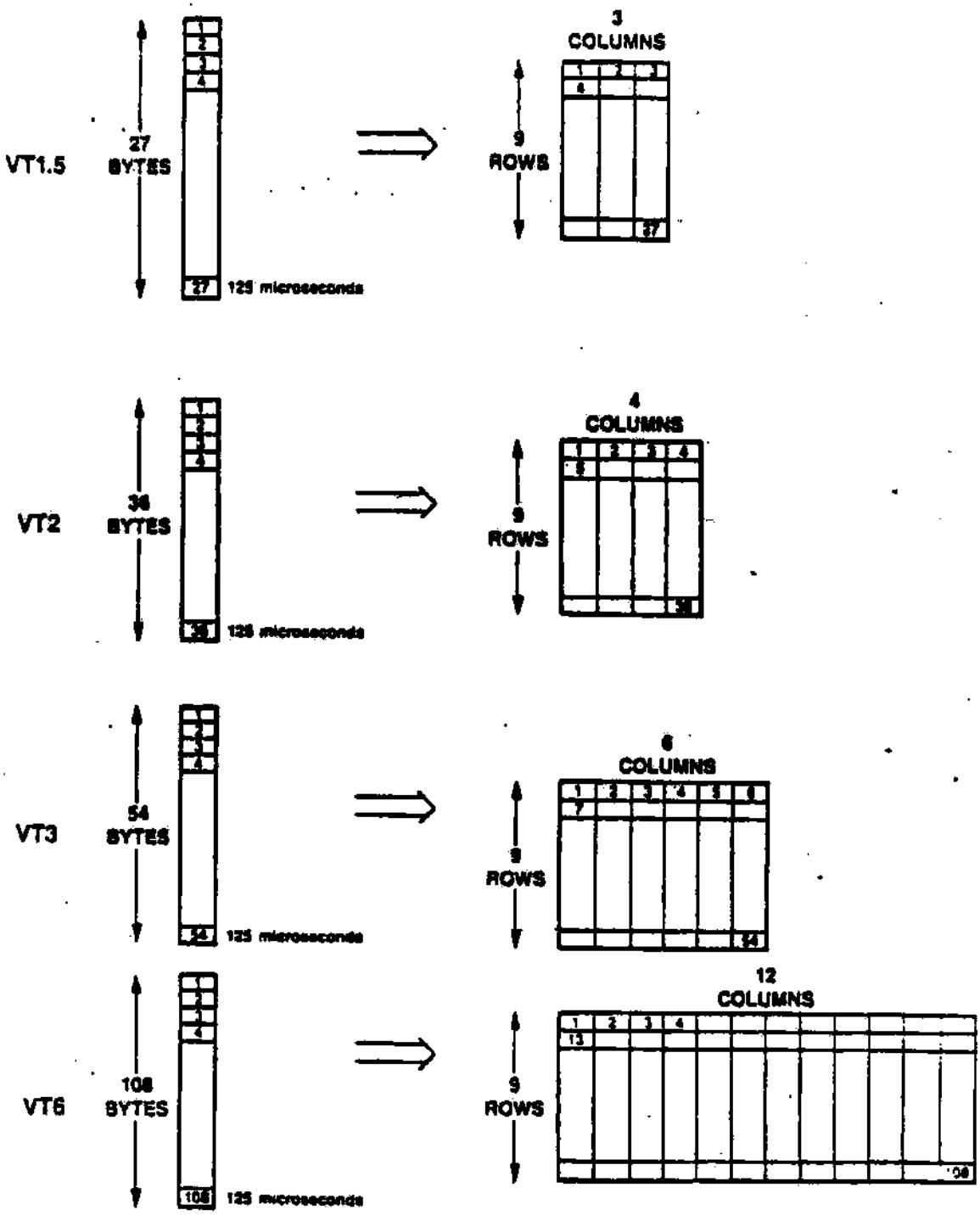


FIGURE 9 – VT SIZES

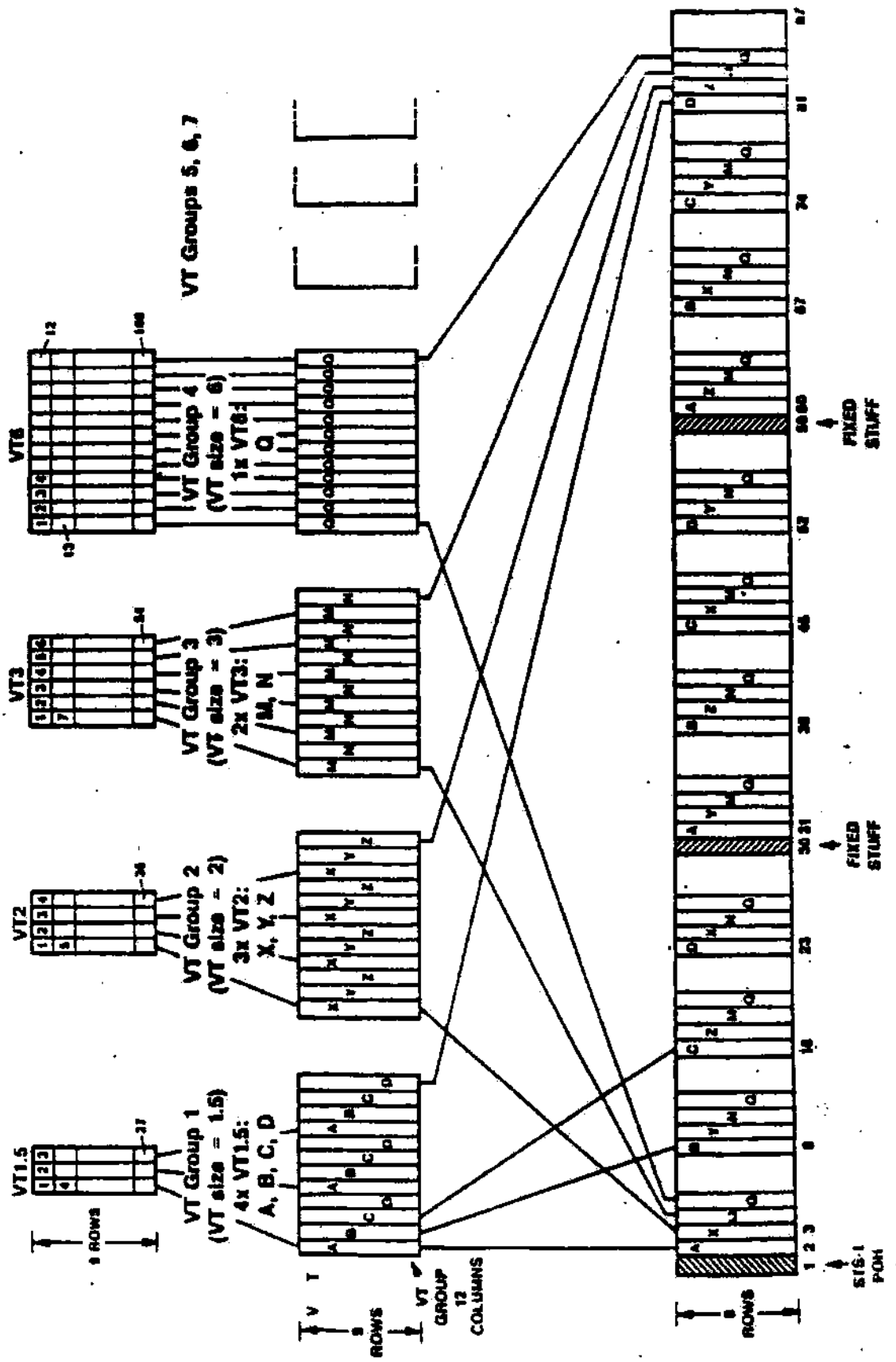


FIGURE 10 – Example of VT Structured STS-1 SPE

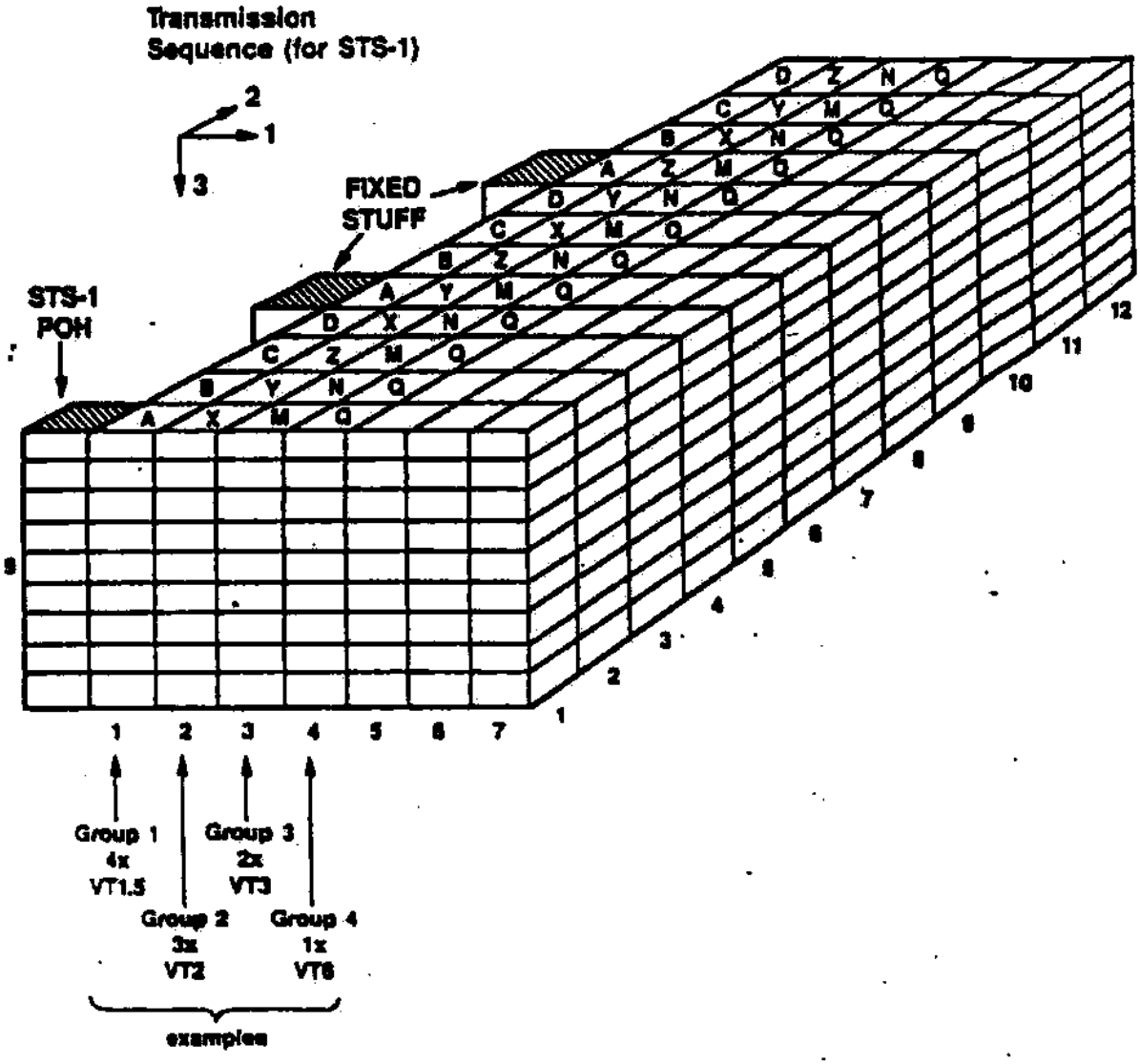


FIGURE 11 – 3-dimensional representation of example VT-structured STS-1 SPE

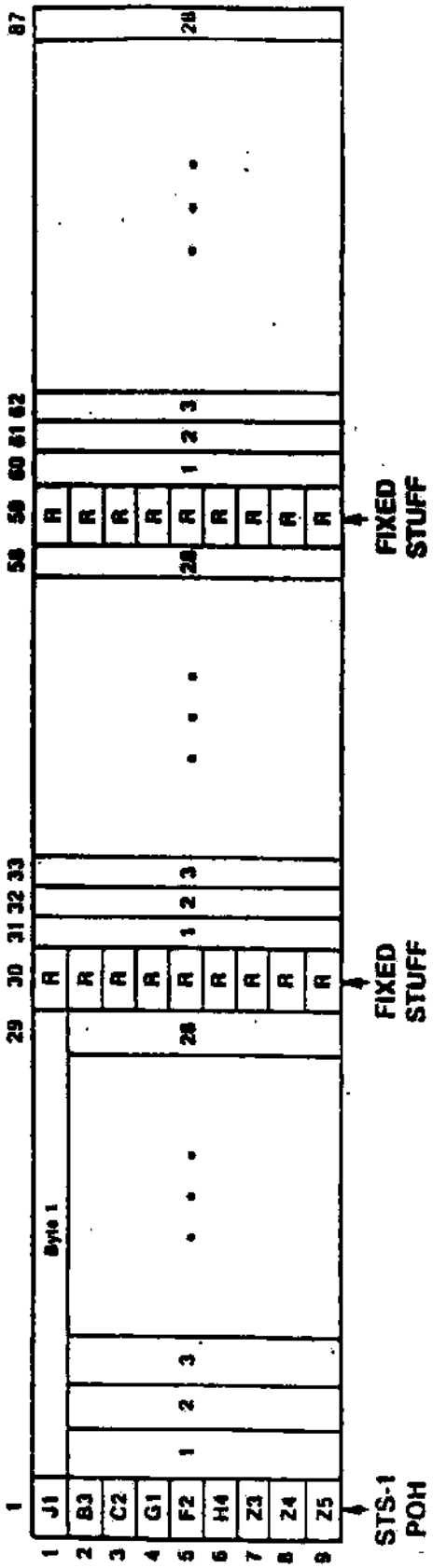


FIGURE 12 – VT STRUCTURED STS-1 SPE: ALL VT1.5

VT1.5 #	GROUP #/VT #	COLUMN #s
1	1, 1	2, 31, 60
2	2, 1	3, 32, 61
3	3, 1	4, 33, 62
4	4, 1	5, 34, 63
5	5, 1	6, 35, 64
6	6, 1	7, 36, 65
7	7, 1	8, 37, 66
8	1, 2	9, 38, 67
9	2, 2	10, 39, 68
10	3, 2	11, 40, 69
11	4, 2	12, 41, 70
12	5, 2	13, 42, 71
13	6, 2	14, 43, 72
14	7, 2	15, 44, 73
15	1, 3	16, 45, 74
16	2, 3	17, 46, 75
17	3, 3	18, 47, 76
18	4, 3	19, 48, 77
19	5, 3	20, 49, 78
20	6, 3	21, 50, 79
21	7, 3	22, 51, 80
22	1, 4	23, 52, 81
23	2, 4	24, 53, 82
24	3, 4	25, 54, 83
25	4, 4	26, 55, 84
26	5, 4	27, 56, 85
27	6, 4	28, 57, 86
28	7, 4	29, 58, 87

Column 1 = STS-1 POH
30 = Fixed Stuff
59 = Fixed Stuff

FIGURE 13 – VT1.5 LOCATIONS

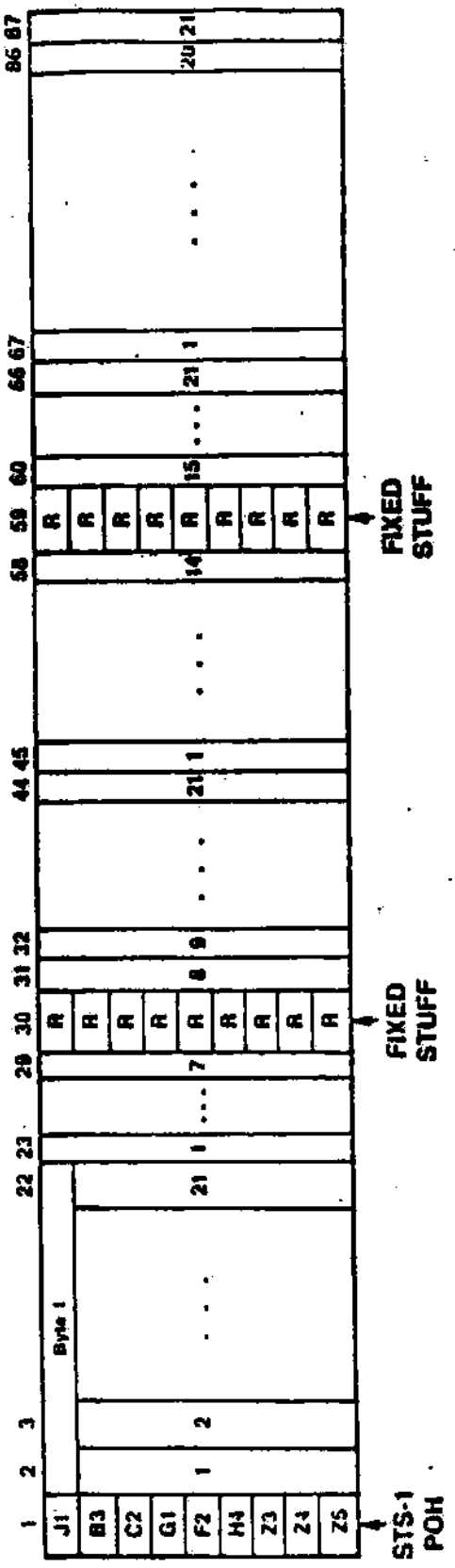


FIGURE 14 – VT Structured STS-1 SPE: ALL VT2

VT2 #	GROUP #/VT #	COLUMN #s
1	1, 1	2, 23, 45, 67
2	2, 1	3, 24, 46, 68
3	3, 1	4, 25, 47, 69
4	4, 1	5, 26, 48, 70
5	5, 1	6, 27, 49, 71
6	6, 1	7, 28, 50, 72
7	7, 1	8, 29, 51, 73
8	1, 2	9, 31, 52, 74
9	2, 2	10, 32, 53, 75
10	3, 2	11, 33, 54, 76
11	4, 2	12, 34, 55, 77
12	5, 2	13, 35, 56, 78
13	6, 2	14, 36, 57, 79
14	7, 2	15, 37, 58, 80
15	1, 3	16, 38, 60, 81
16	2, 3	17, 39, 61, 82
17	3, 3	18, 40, 62, 83
18	4, 3	19, 41, 63, 84
19	5, 3	20, 42, 64, 85
20	6, 3	21, 43, 65, 86
21	7, 3	22, 44, 66, 87

Column 1 = STS-1 POH
30 = Fixed Stuff
59 = Fixed Stuff

Note: Underlined numbers indicate that the following column is fixed stuff.

FIGURE 15 – VT2 LOCATIONS

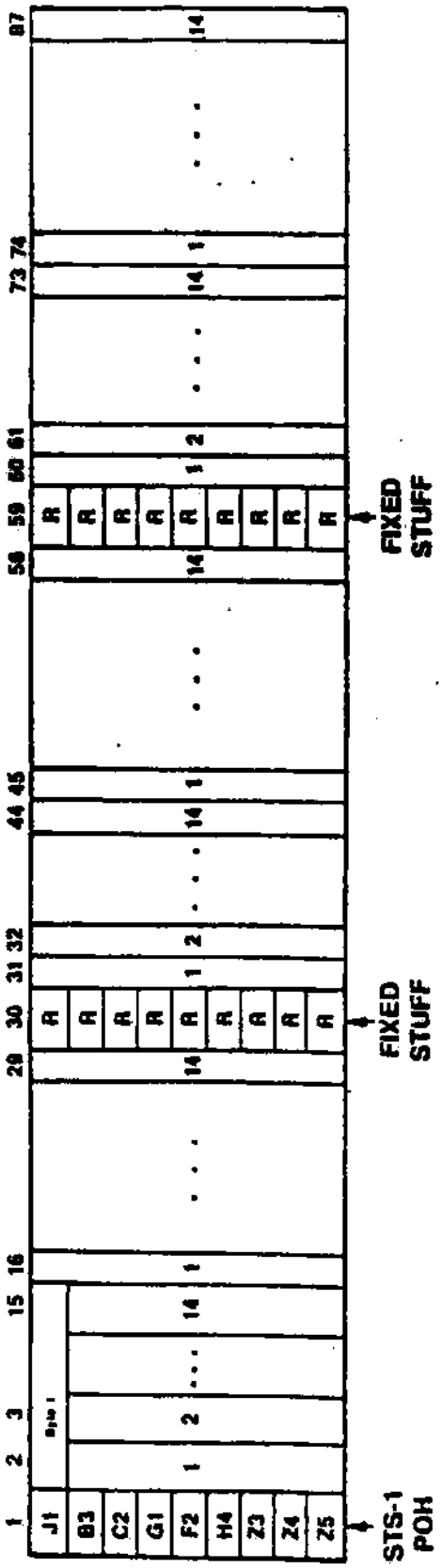


FIGURE 16 – VT STRUCTURED STS-1 SPE: ALL VT3

VT3 #	GROUP #/VT #	COLUMN #s
1	1, 1	2, 16, 31, 45, 60, 74
2	2, 1	3, 17, 32, 46, 61, 75
3	3, 1	4, 18, 33, 47, 62, 76
4	4, 1	5, 19, 34, 48, 63, 77
5	5, 1	6, 20, 35, 49, 64, 78
6	6, 1	7, 21, 36, 50, 65, 79
7	7, 1	8, 22, 37, 51, 66, 80
8	1, 2	9, 23, 38, 52, 67, 81
9	2, 2	10, 24, 39, 53, 68, 82
10	3, 2	11, 25, 40, 54, 69, 83
11	4, 2	12, 26, 41, 55, 70, 84
12	5, 2	13, 27, 42, 56, 71, 85
13	6, 2	14, 28, 43, 57, 72, 86
14	7, 2	15, 29, 44, 58, 73, 87

Column 1 = STS-1 POH
30 = Fixed Stuff
59 = Fixed Stuff

FIGURE 17 – VT3 LOCATIONS

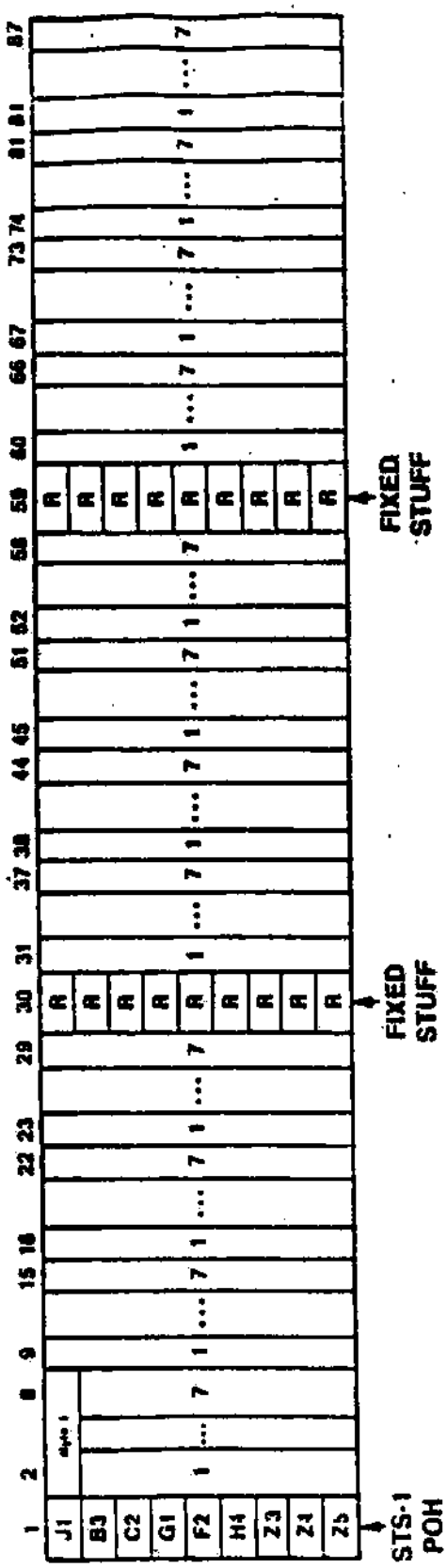


FIGURE 18 – VT STRUCTURED STS-1 SPE: ALL VT6

VT6 #	GROUP #/VT #	COLUMN #s
1	1, 1	2, 9, 16, 23, 31, 38, 45, 52, 60, 67, 74, 81
2	2, 1	3, 10, 17, 24, 32, 39, 46, 53, 61, 68, 75, 82
3	3, 1	4, 11, 18, 25, 33, 40, 47, 54, 62, 69, 76, 83
4	4, 1	5, 12, 19, 26, 34, 41, 48, 55, 63, 70, 77, 84
5	5, 1	6, 13, 20, 27, 35, 42, 49, 56, 64, 71, 78, 85
6	6, 1	7, 14, 21, 28, 36, 43, 50, 57, 65, 72, 79, 86
7	7, 1	8, 15, 22, 29, 37, 44, 51, 58, 66, 73, 80, 87

Column 1 = STS-1 POH
30 = Fixed Stuff
59 = Fixed Stuff

FIGURE 19 – VT6 LOCATIONS

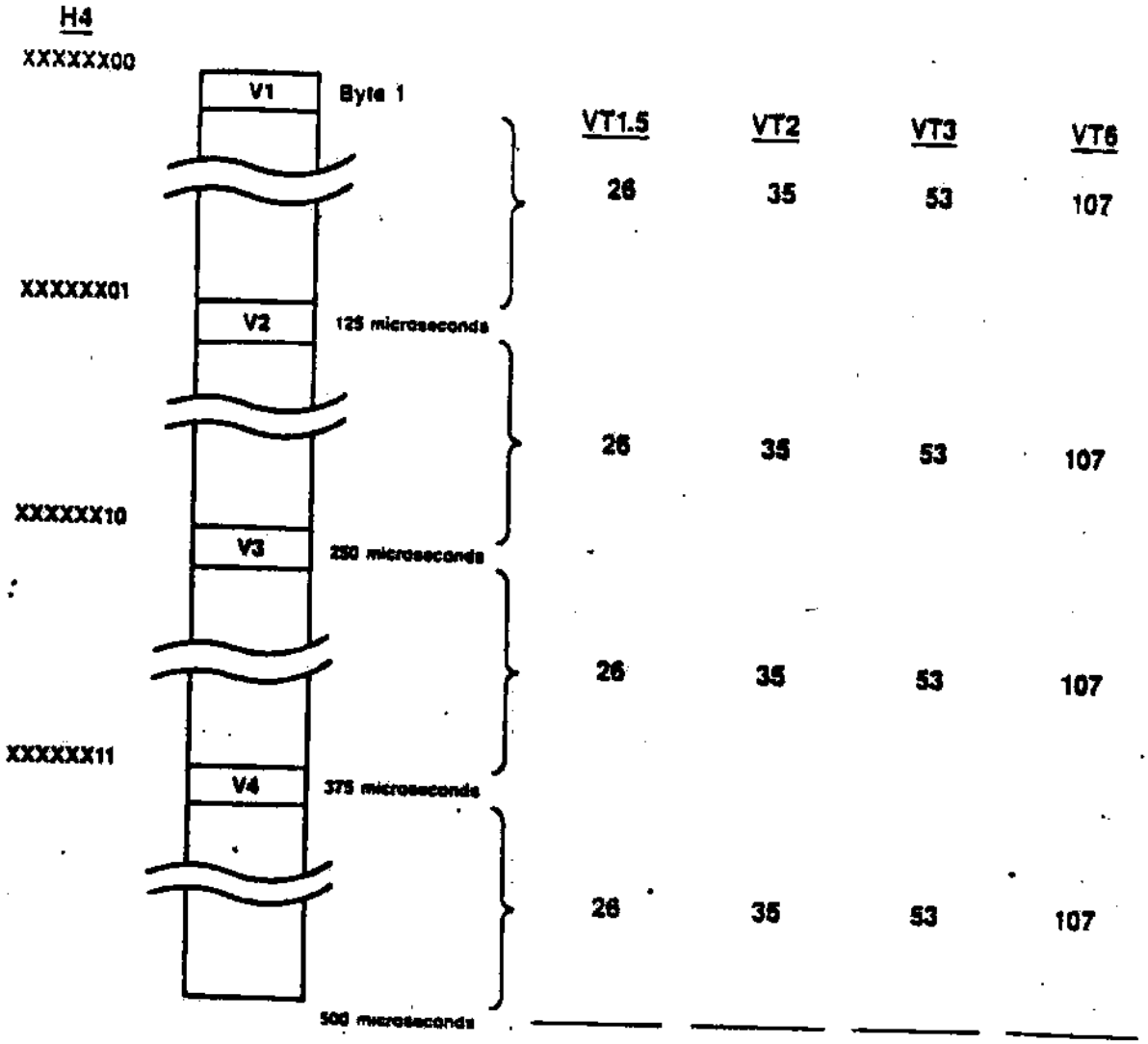
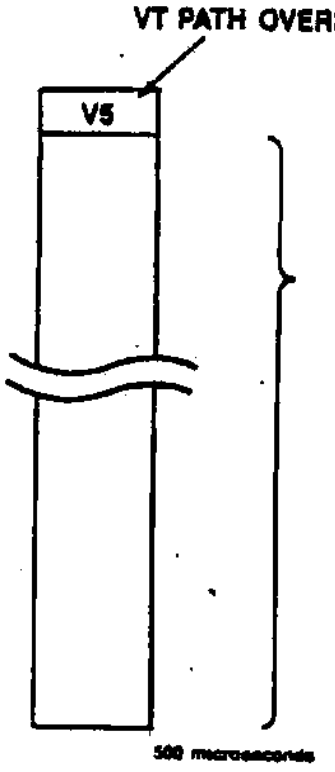


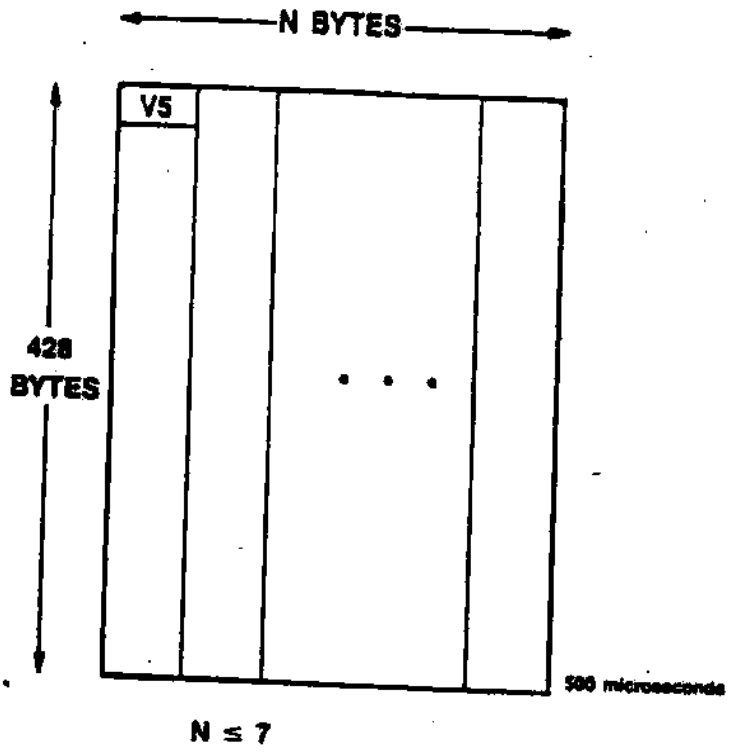
FIGURE 20 – VT Superframe



VT PAYLOAD CAPACITY (BYTES/500 microseconds)

VT1.5	VT2	VT3	VT6
103	139	211	427

FIGURE 21 – VT Synchronous Payload Envelope



Payload Capacity = (N × 428) − 1 Bytes/500 microseconds

FIGURE 22 – VT6-Nc SPE

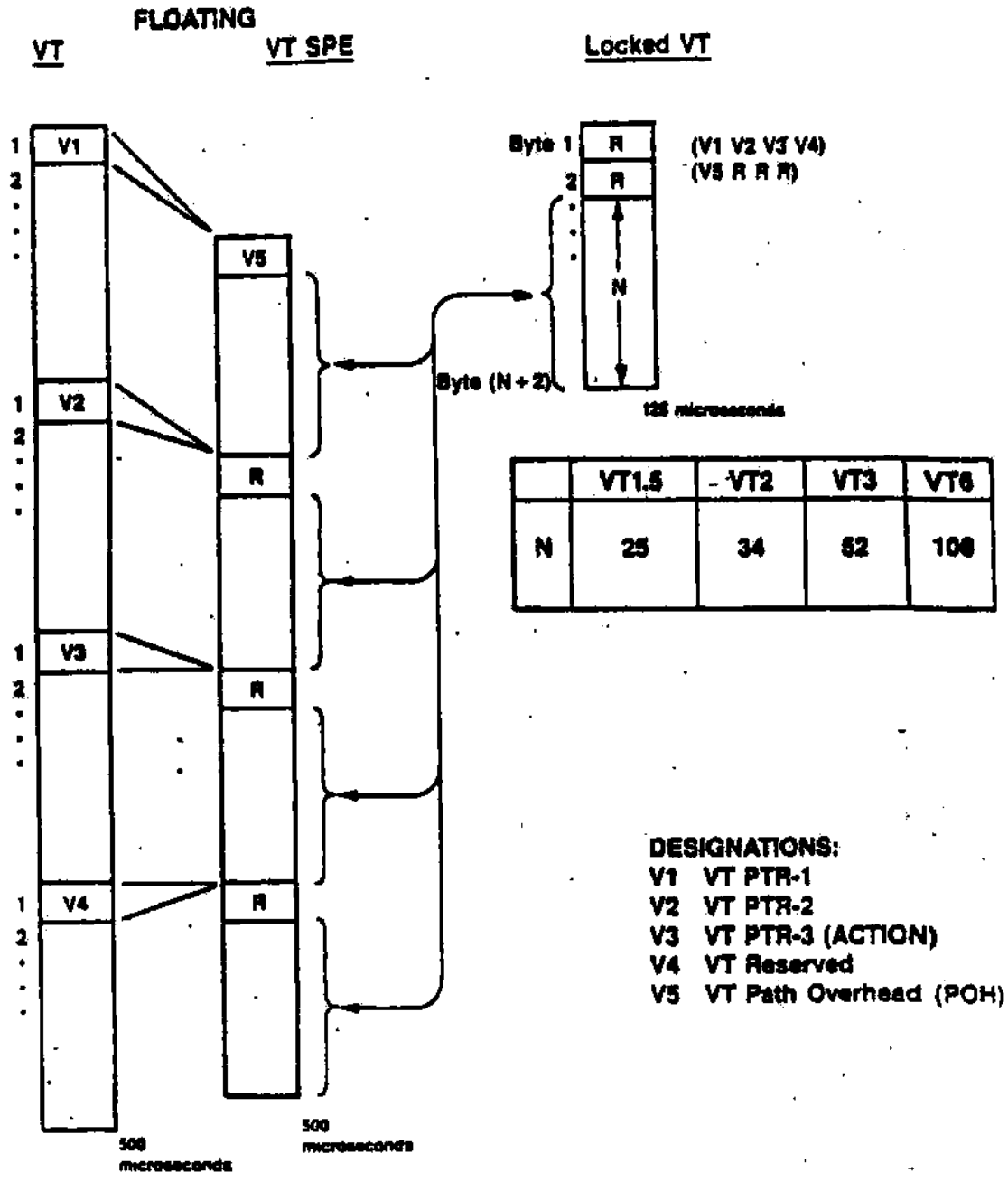


FIGURE 23 – CONVERSION BETWEEN FLOATING AND LOCKED VT MODES

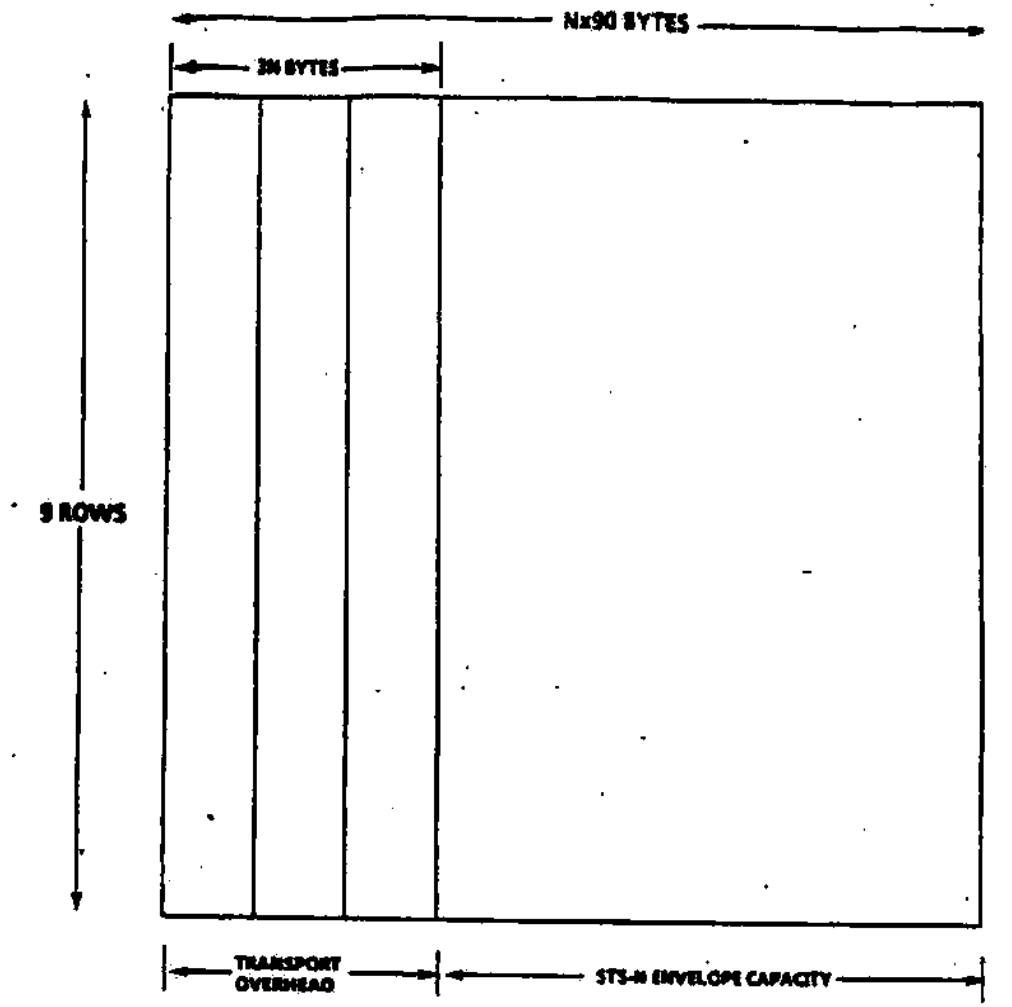


FIGURE 24 STS-N FRAME

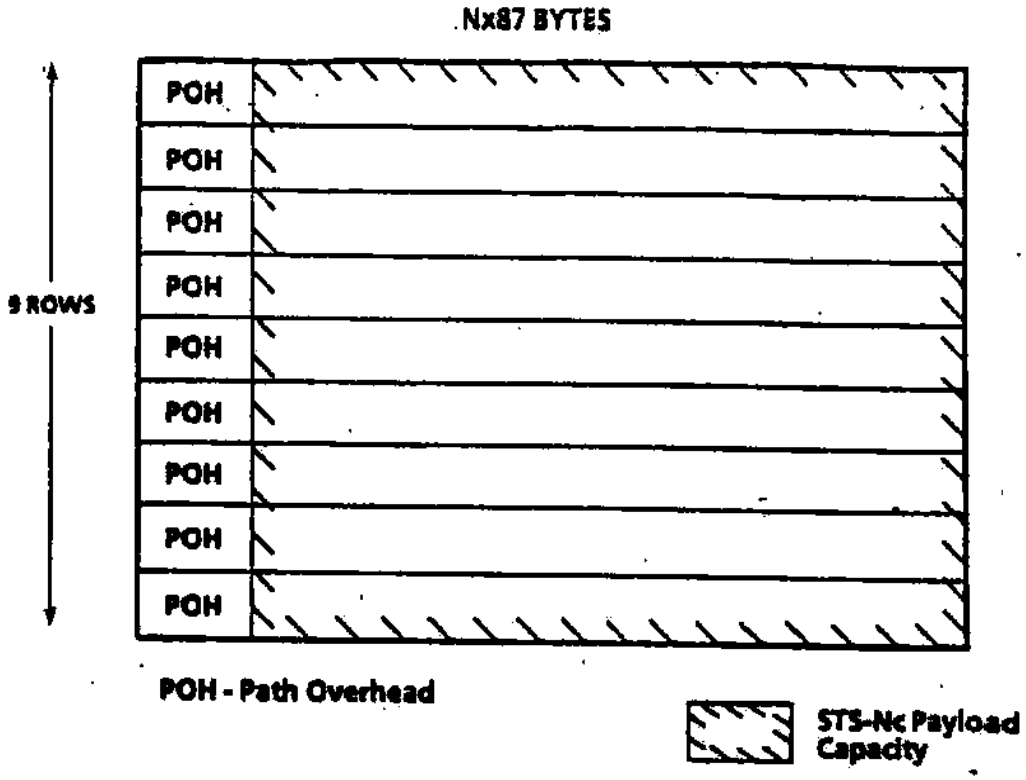


FIGURE 25 STS-Nc Synchronous Payload Envelope

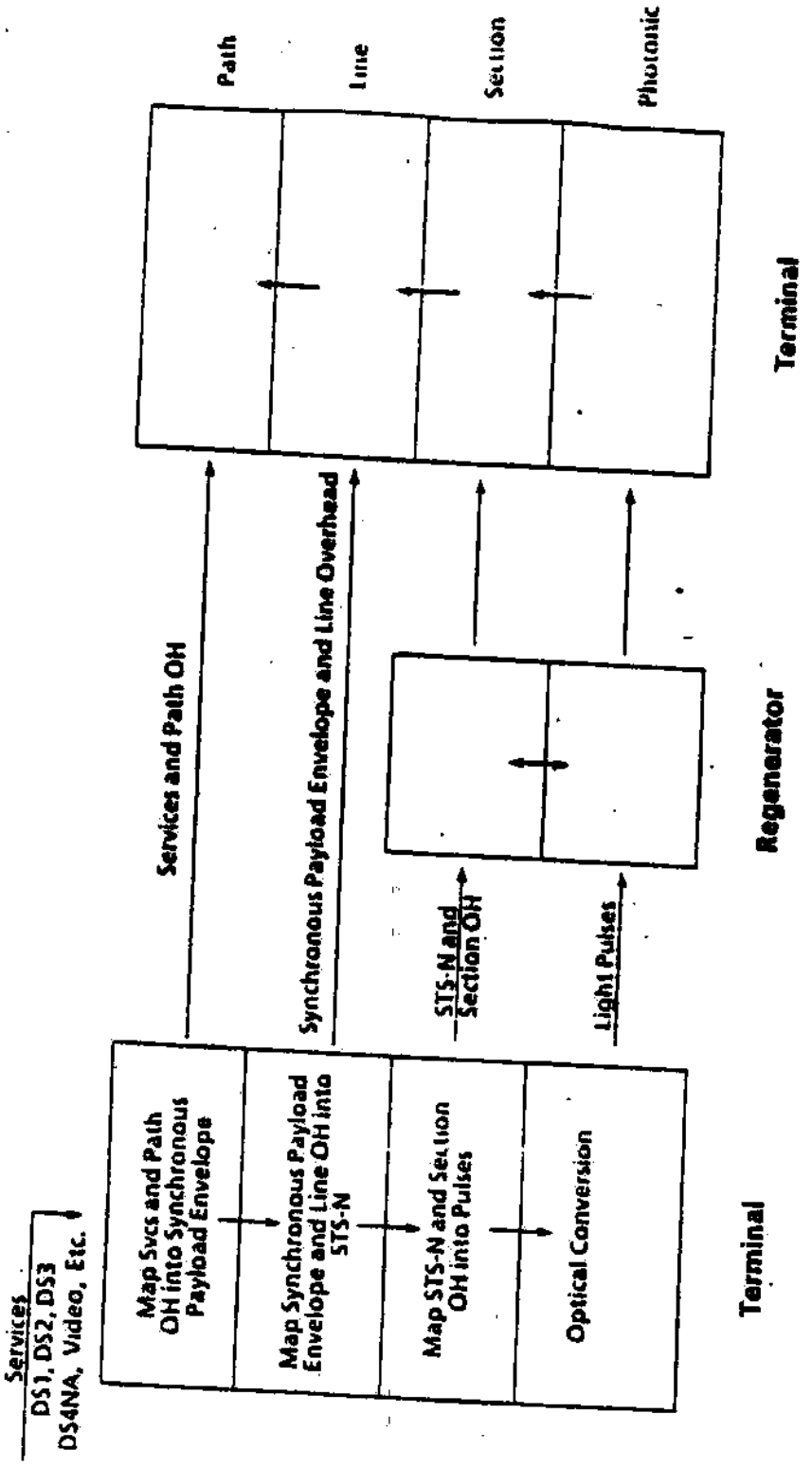


FIGURE 26 - Optical Interface Layers

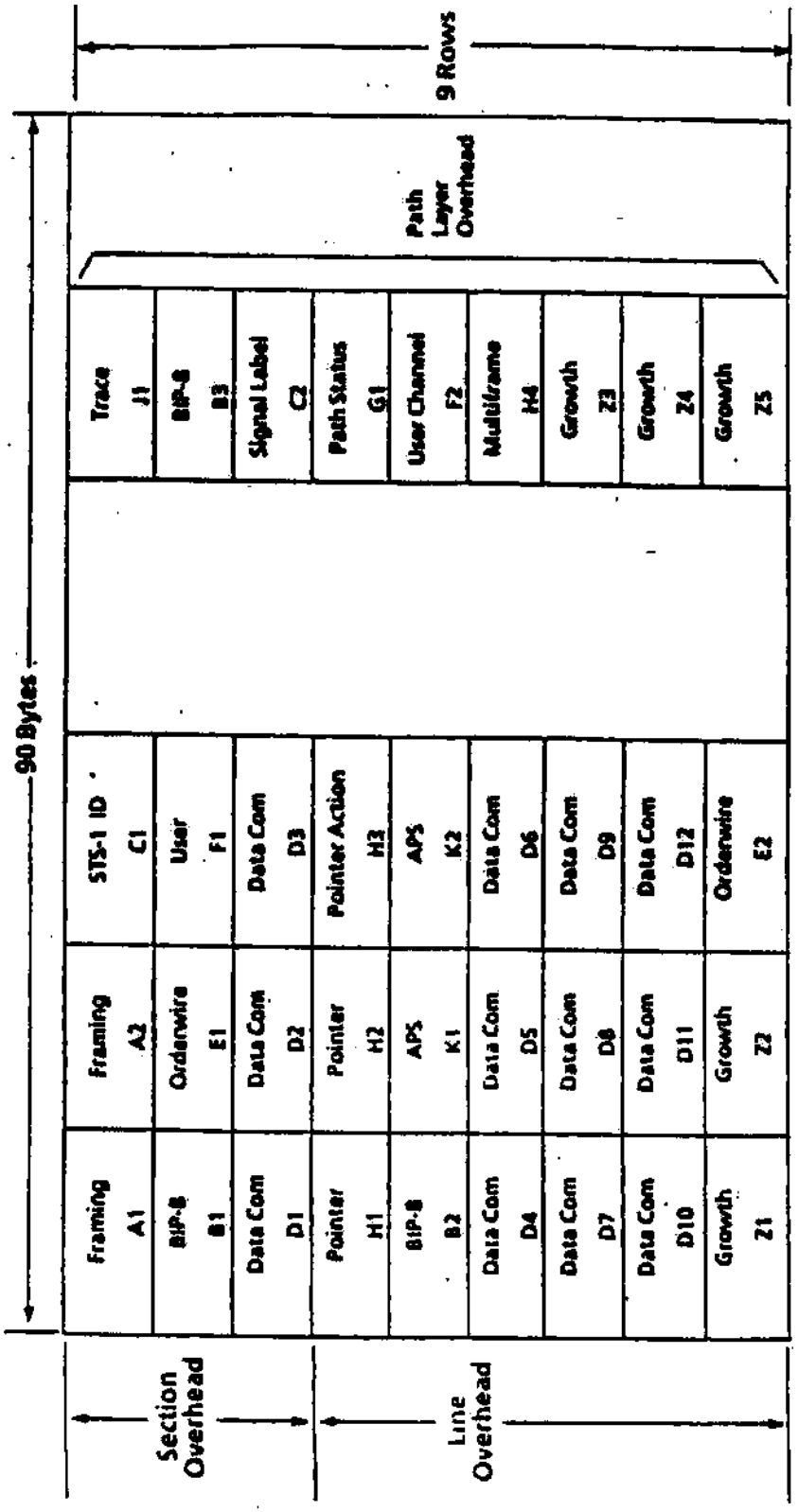


FIGURE 27 - Overhead Byte Locations in an STS-1 Frame

STS PATH FEBE CODING:

0 0 0 0	0 ERRORS
0 0 0 1	1 ERROR
•	
•	
•	
0 1 1 1	7 ERRORS
1 0 0 0	8 ERRORS
1 0 0 1	
•	
•	0 ERRORS
•	
1 1 1 1	

FIGURE 28 - STS PATH STATUS (G1)

VT PATH SIGNAL LABEL CODING:

0 0 0	UNEQUIPPED
0 0 1	EQUIPPED-NONSPECIFIC
0 1 0	EQUIPPED-(CURRENTLY UNASSIGNED)
•	
•	
•	
1 1 0	
1 1 1	AIS

FIGURE 29 - VT PATH OVERHEAD (V5)

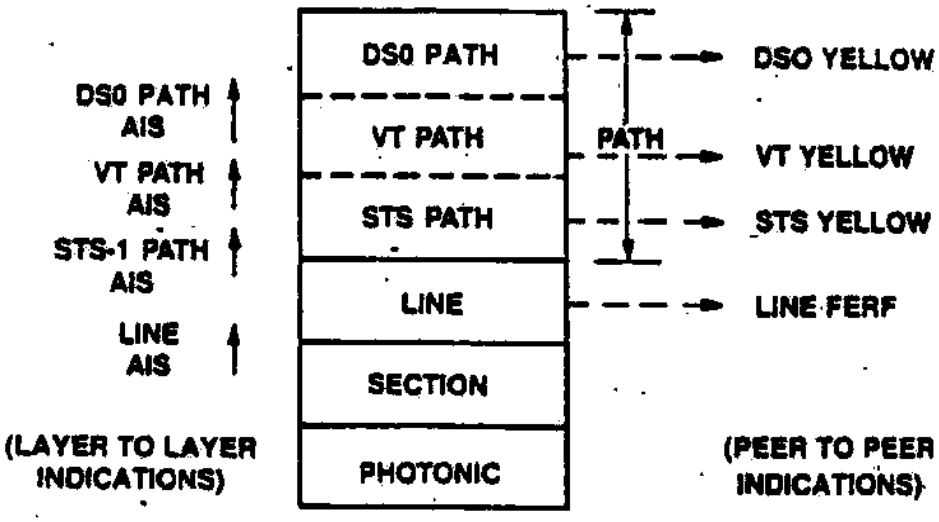
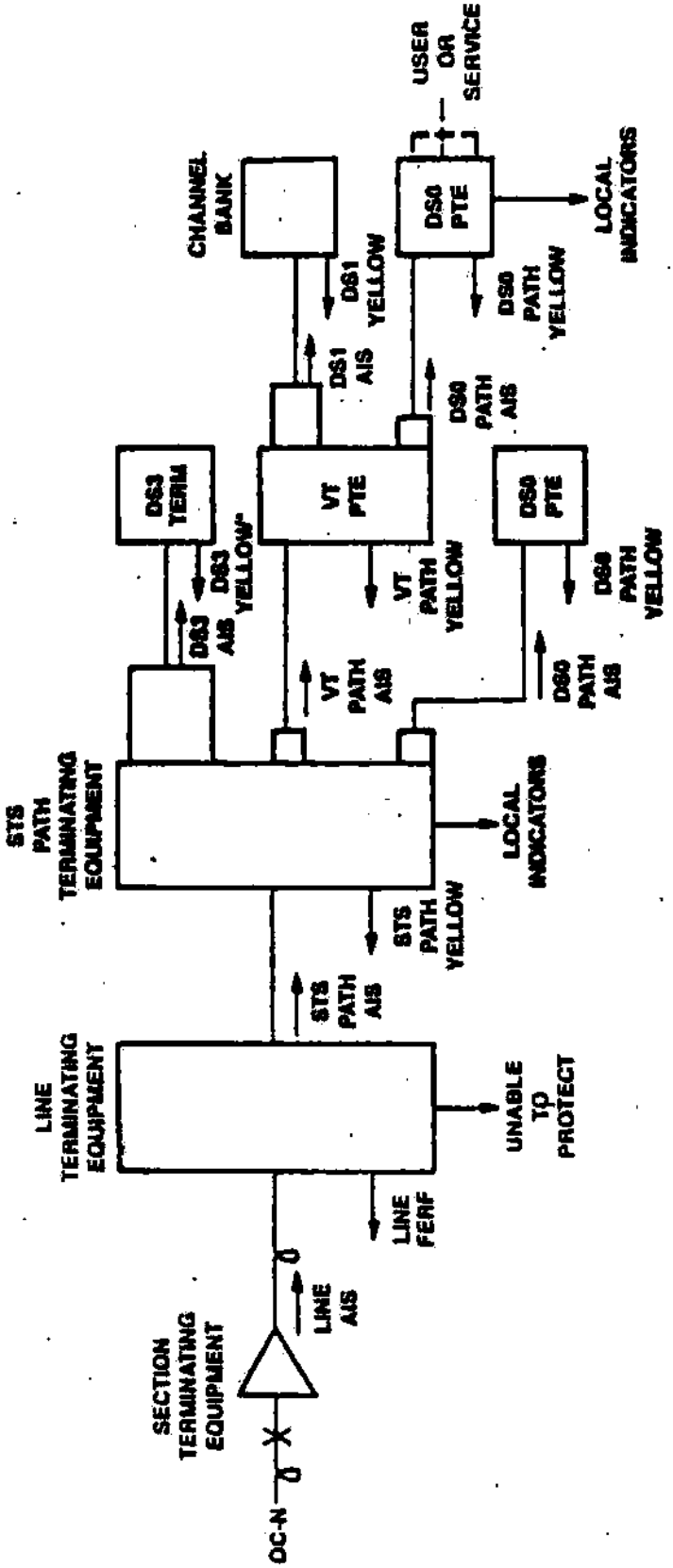
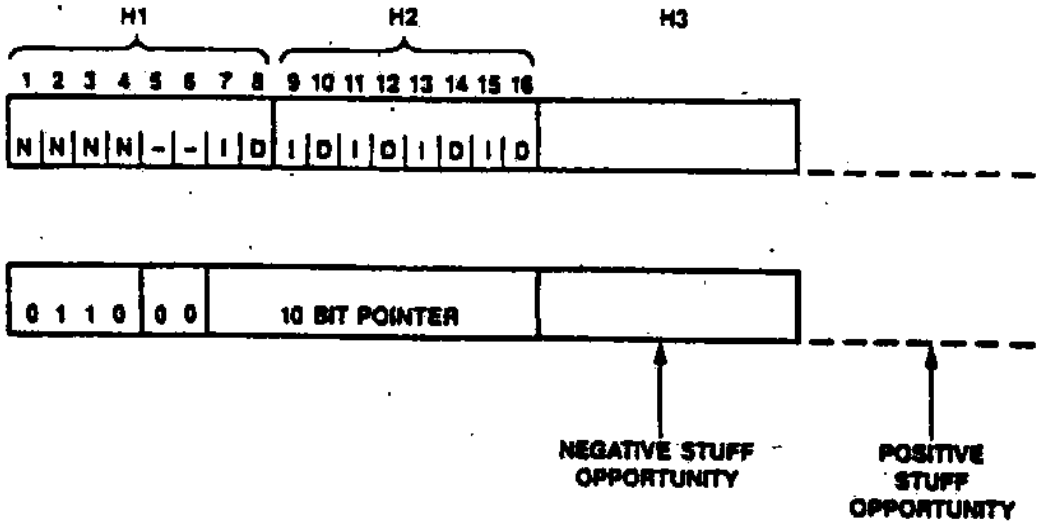


FIGURE 30 – LAYERED MODEL REPRESENTATION OF AIS, YELLOW, AND FERF INDICATIONS



*SEE REFERENCE 3 FOR SPECIFICATION OF DS3 YELLOW.

FIGURE 31 – EQUIPMENT EXAMPLES OF AIS AND YELLOW INDICATIONS



NEW DATA FLAG:
Invert 4 N Bits
Accept exact match (suggested implementation)

NEGATIVE STUFF:
Invert 5 D Bits
Accept Majority Vote (suggested implementation)

POSITIVE STUFF:
Invert 5 I Bits
Accept Majority Vote (suggested implementation)

I – Increment Bit
D – Decrement Bit
N – New Data Flag Bit

FIGURE 32 – STS-1 PAYLOAD POINTER (H1, H2, H3) CODING

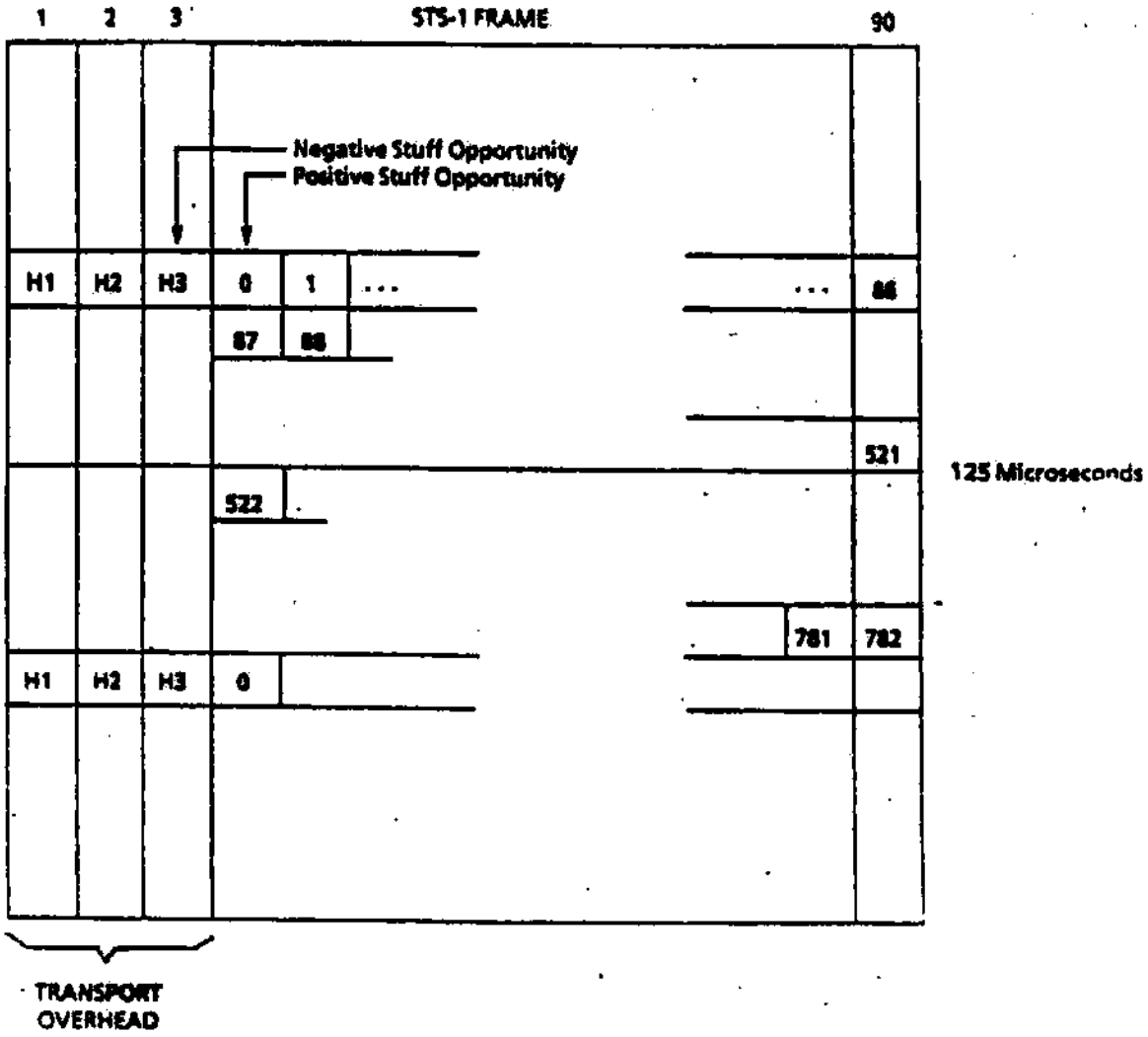


FIGURE 33- STS-1 Pointer Offset Numbering

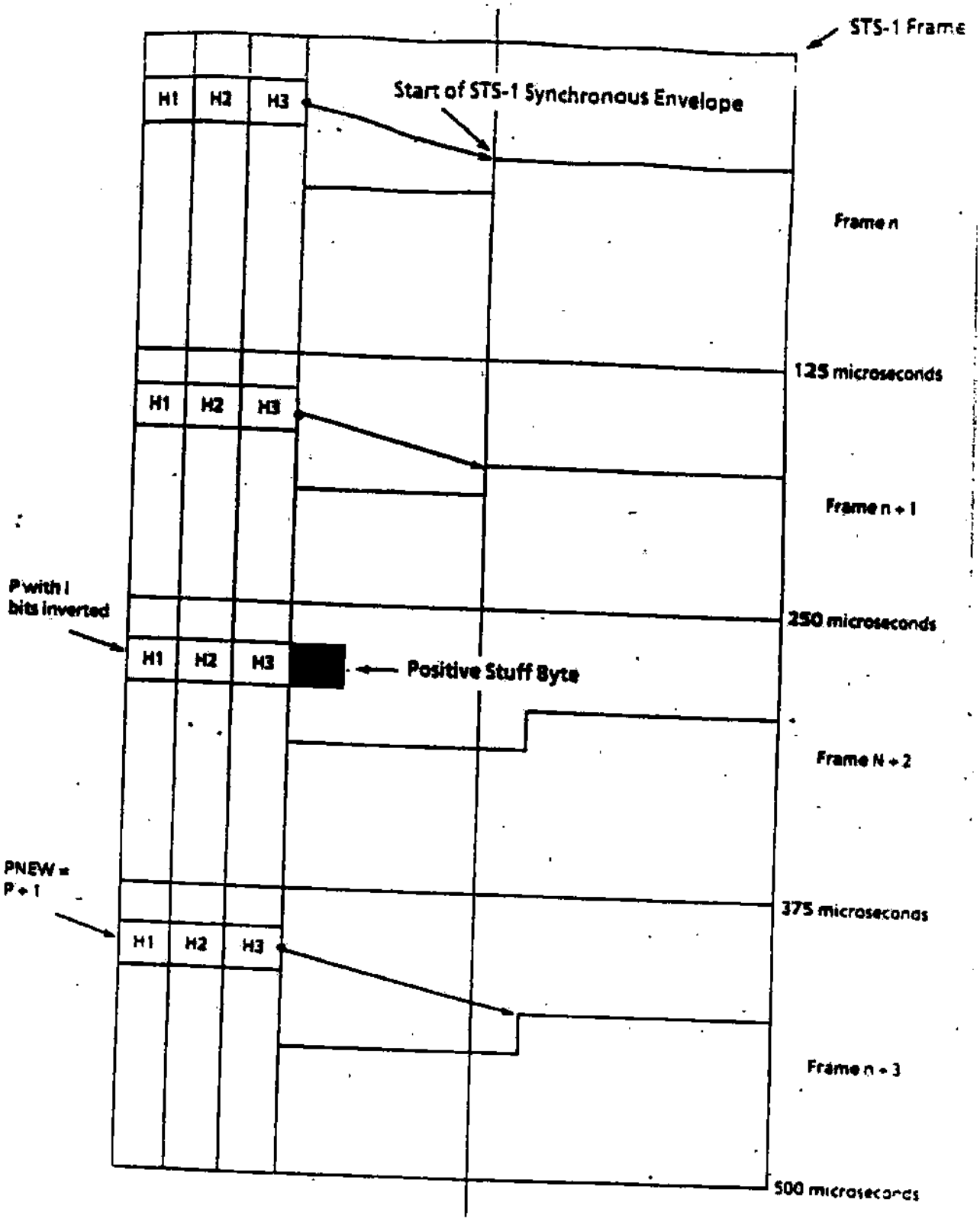


FIGURE 34- Positive STS - 1 Pointer Adjustment Operation

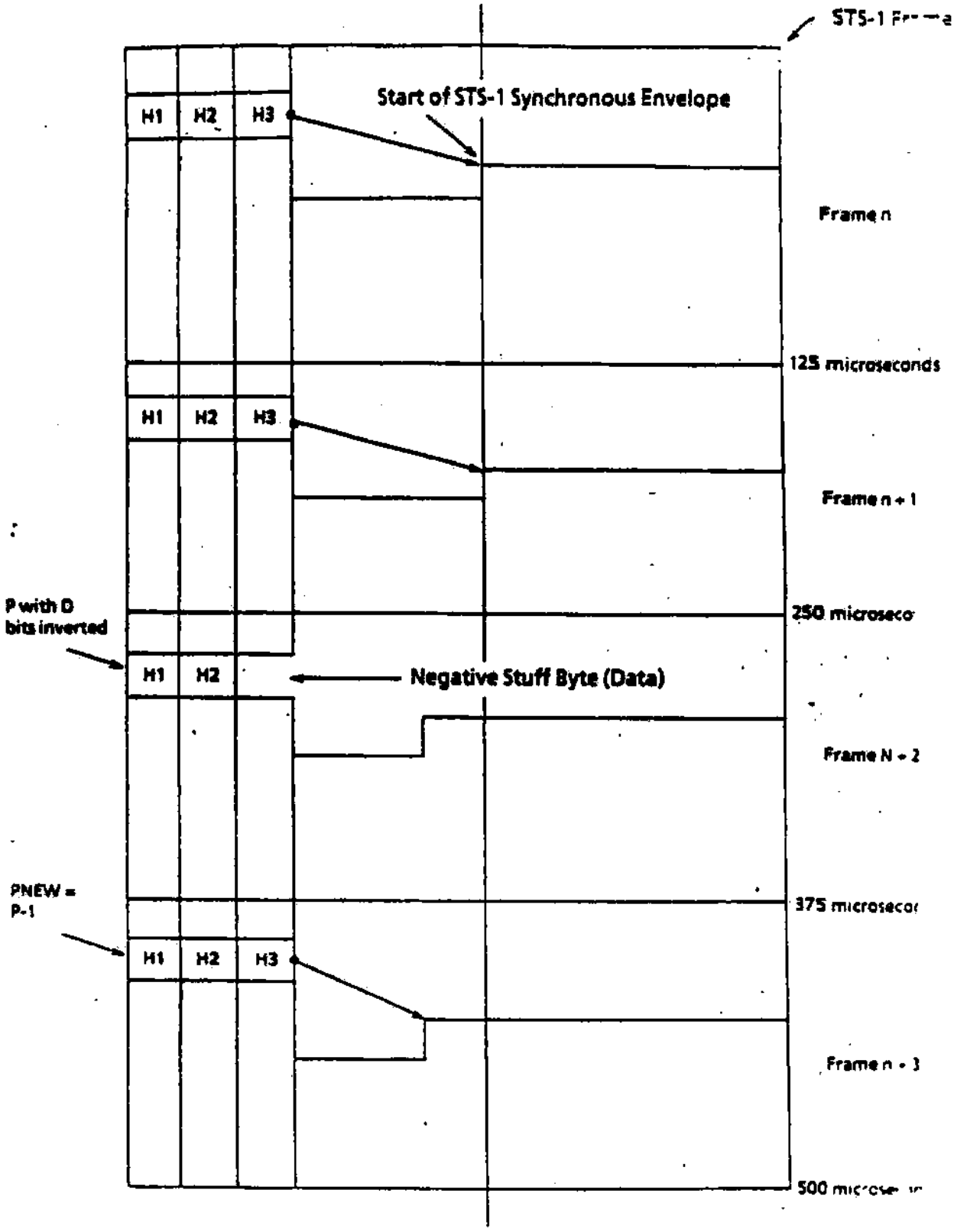
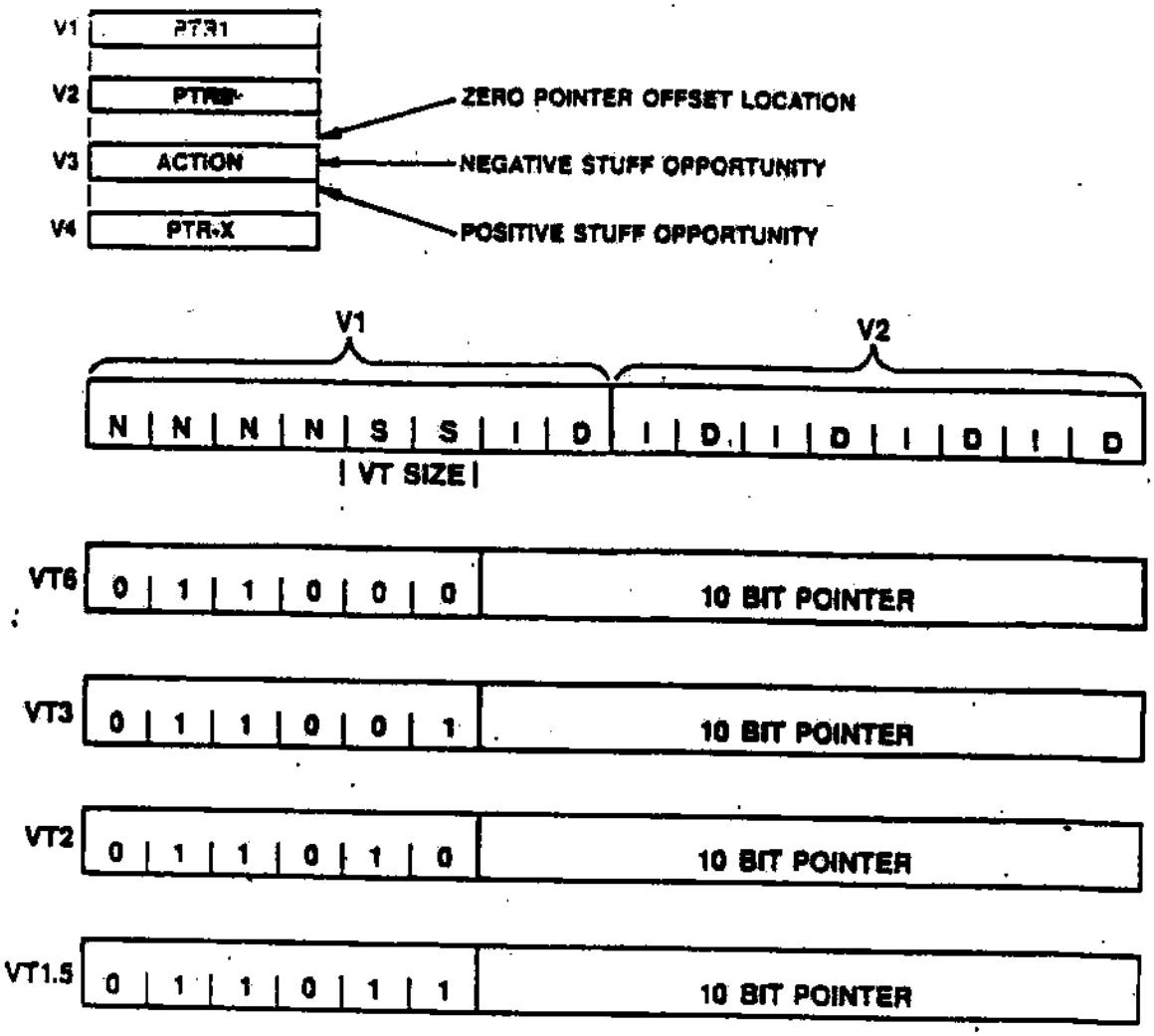
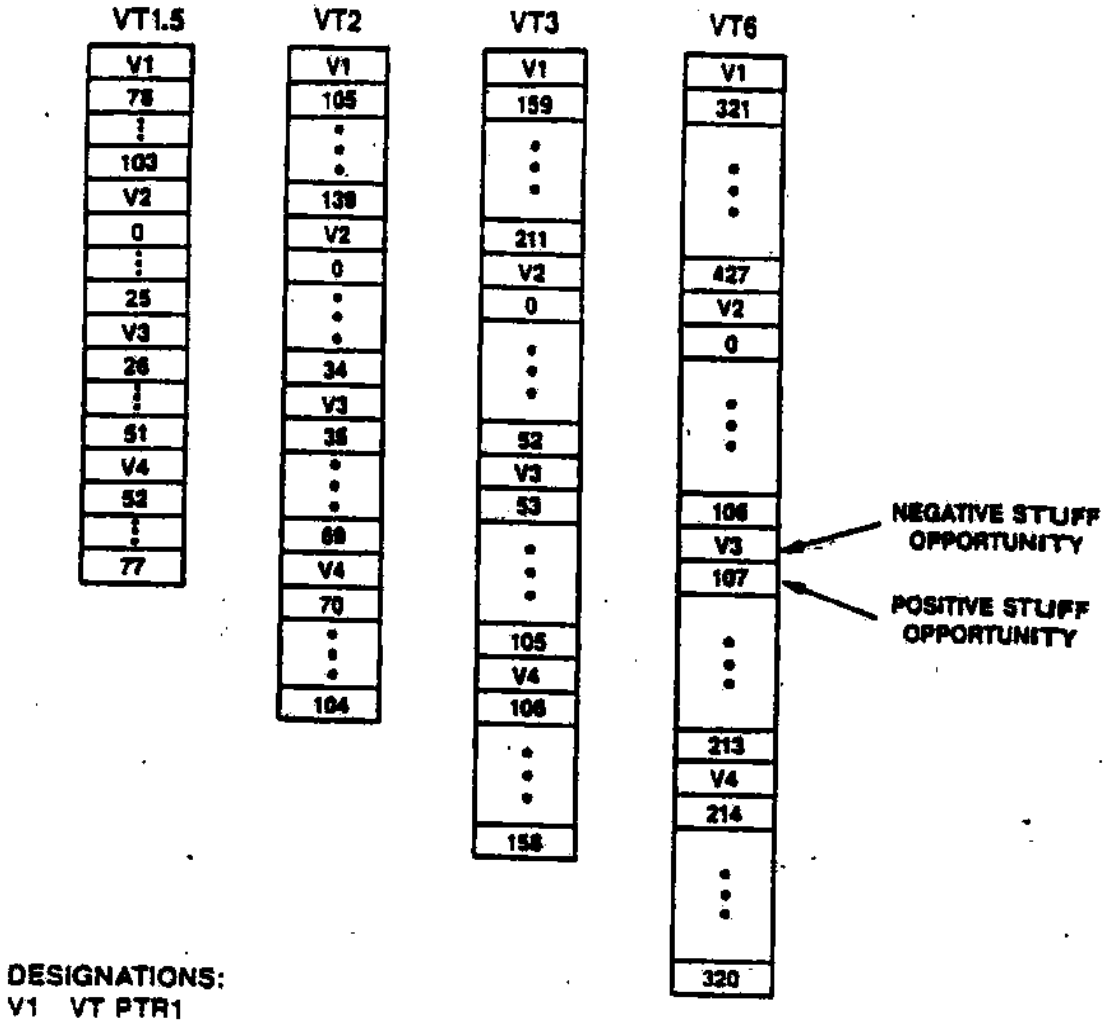


FIGURE 35- Negative STS - 1 Pointer Adjustment Operation



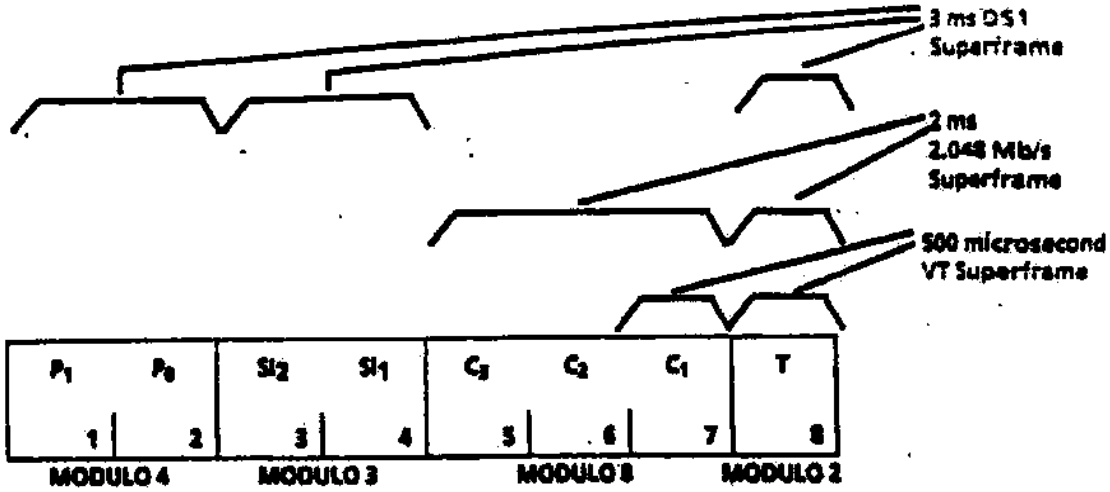
NEW DATA FLAG – INVERT 4 N BITS – ACCEPT EXACT MATCH
NEGATIVE STUFF – INVERT 5 D BITS – ACCEPT MAJORITY VOTE
POSITIVE STUFF – INVERT 5 I BITS – ACCEPT MAJORITY VOTE
} (SUGGESTED IMPLEMENTATION)

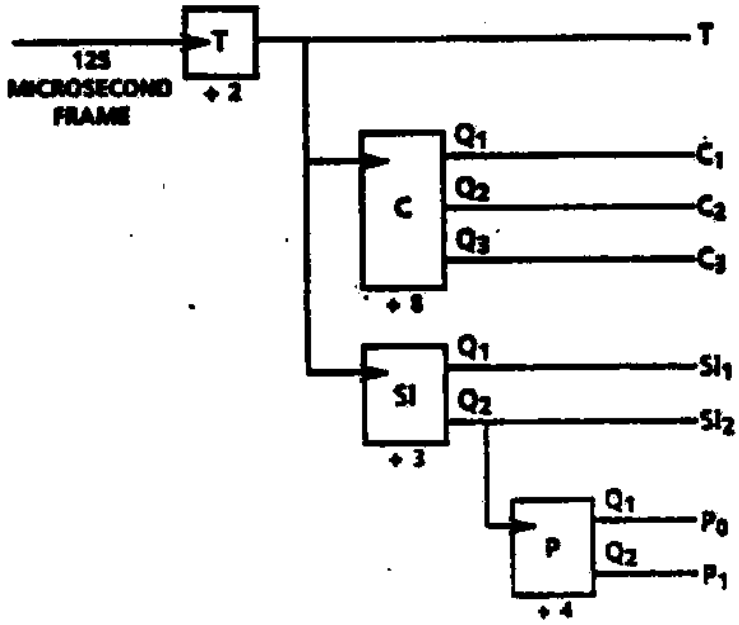
FIGURE 36 – VT PAYLOAD POINTER CODING



DESIGNATIONS:
V1 VT PTR1
V2 VT PTR2
V3 VT PTR3 (ACTION)
V4 VT RESERVED

FIGURE 37 – VT POINTER OFFSETS





NOTE: BLOCK DIAGRAM FOR FUNCTIONAL CLARIFICATION ONLY. THIS IS NOT A RECOMMENDATION AS TO IMPLEMENTATION.

FIGURE 38 - VT MULTIFRAME INDICATOR BYTE (H4)

FULL H4 CODING SEQUENCE: MANDATORY IN LOCKED VT MODE. OPTIONAL IN FLOATING VT MODE.

BIT: 1 2	3 4	5 6 7	8	FRAMES	TIME
					0
0 0	0 0	0 0 0	0	0	
0 0	0 0	0 0 0	1	1	
0 0	0 1	0 0 1	0	2	
0 0	0 1	0 0 1	1	3	500 microsecond VT superframe
0 0	1 0	0 1 0	0	4	
0 0	1 0	0 1 0	1	5	
0 1	0 0	0 1 1	0	6	
0 1	0 0	0 1 1	1	7	
0 1	0 1	1 0 0	0	8	
0 1	0 1	1 0 0	1	9	
0 1	1 0	1 0 1	0	10	
0 1	1 0	1 0 1	1	11	
1 0	0 0	1 1 0	0	12	
1 0	0 0	1 1 0	1	13	
1 0	0 1	1 1 1	0	14	
1 0	0 1	1 1 1	1	15	2ms 2.048 Mb/s signalling cycle
1 0	1 0	0 0 0	0	16	
1 0	1 0	0 0 0	1	17	
1 1	0 0	0 0 1	0	18	
1 1	0 0	0 0 1	1	19	
1 1	0 1	0 1 0	0	20	
1 1	0 1	0 1 0	1	21	
1 1	1 0	0 1 1	0	22	
1 1	1 0	0 1 1	1	23	3ms DS1 signalling cycle
0 0	0 0	1 0 0	0	24	
0 0	0 0	1 0 0	1	25	
0 0	0 1	1 0 1	0	26	
0 0	0 1	1 0 1	1	27	
0 0	1 0	1 1 0	0	28	
0 0	1 0	1 1 0	1	29	
0 1	0 0	1 1 1	0	30	
0 1	0 0	1 1 1	1	31	
0 1	0 1	0 0 0	0	32	
0 1	0 1	0 0 0	1	33	
0 1	1 0	0 0 1	0	34	
0 1	1 0	0 0 1	1	35	
1 0	0 0	0 1 0	0	36	
1 0	0 0	0 1 0	1	37	
1 0	0 1	0 1 1	0	38	
1 0	0 1	0 1 1	1	39	
1 0	1 0	1 0 0	0	40	
1 0	1 0	1 0 0	1	41	
1 1	0 0	1 0 1	0	42	
1 1	0 0	1 0 1	1	43	
1 1	0 1	1 1 0	0	44	
1 1	0 1	1 1 0	1	45	
1 1	1 0	1 1 1	0	46	
1 1	1 0	1 1 1	1	47	6ms = cycle repeat time

FIGURE 39 - VT MULTIFRAME INDICATOR BYTE (H4) FULL CODING SEQUENCE

REDUCED H4 CODING SEQUENCE: OPTIONAL IN FLOATING VT MODE.

BIT: 1 2	3 4	5 6 7	8	FRAMES	TIME
					'0'
1 1	1 1	1 1 0	0	0	
1 1	1 1	1 1 0	1	1	
1 1	1 1	1 1 1	0	2	
1 1	1 1	1 1 1	1	3	500 microsecond VT superframe

Note that use of reduced mode can be detected by bits 3 and 4 = '1'.

FIGURE 40 - VT MULTIFRAME INDICATOR BYTE (H4)
REDUCED CODING SEQUENCE

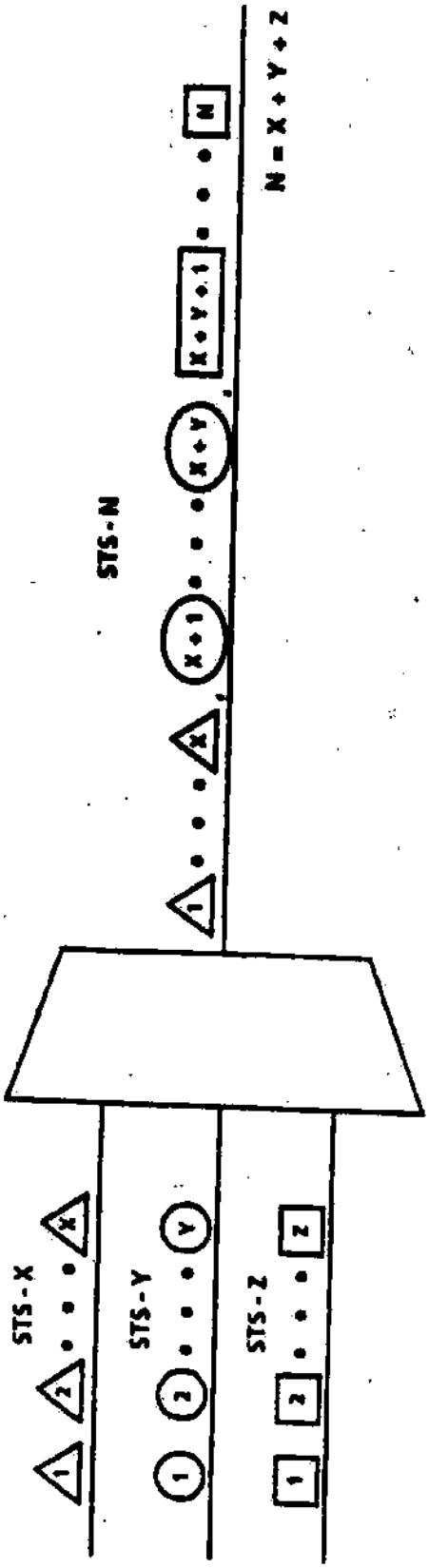


FIGURE 41 - STS-N INTERLEAVING

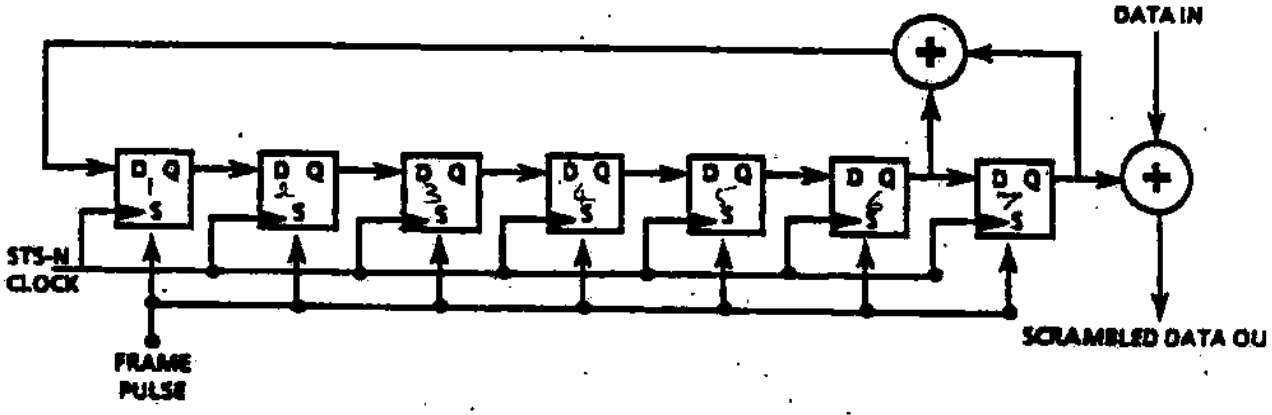
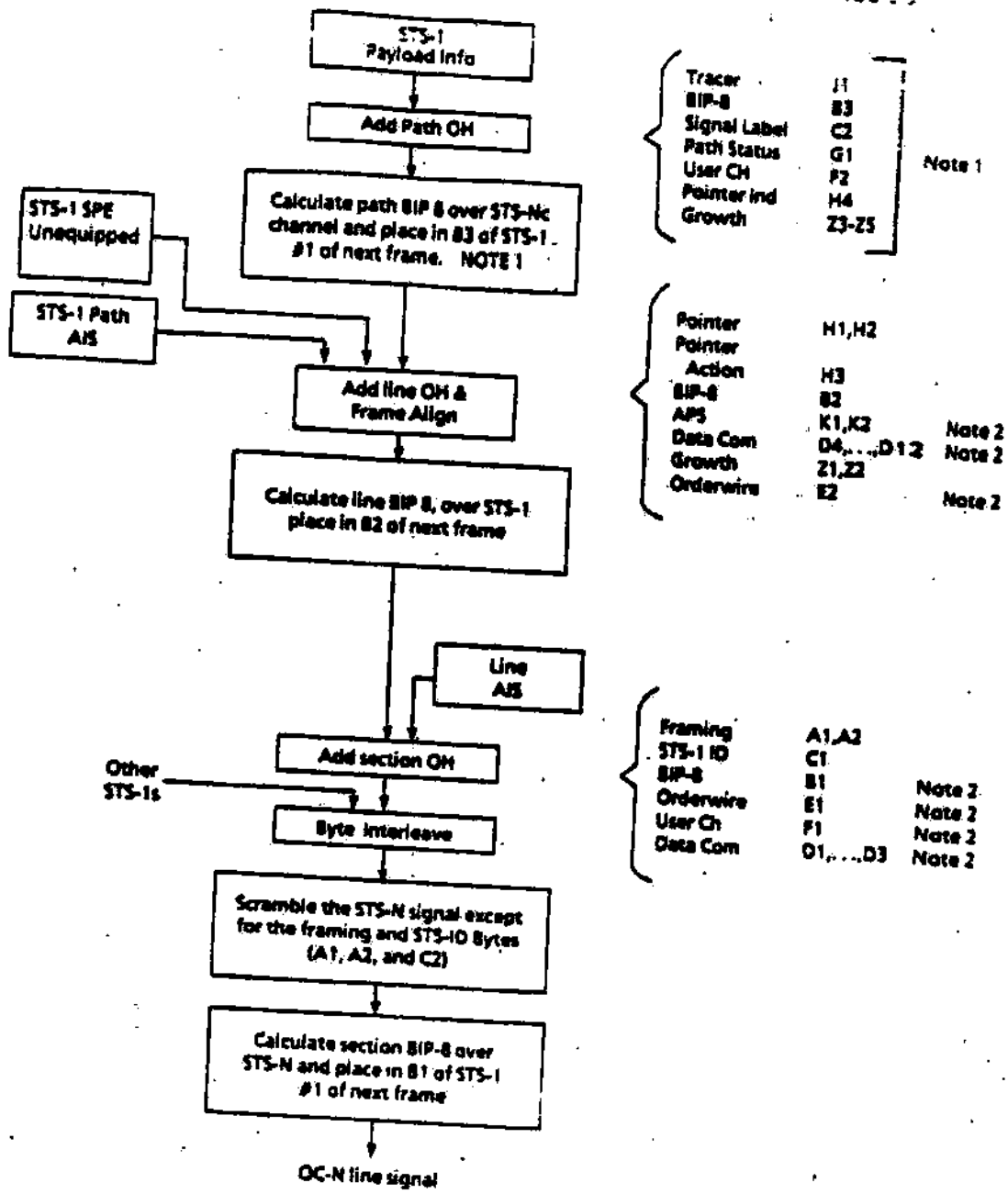


FIGURE 42 - FRAME SYNCHRONOUS SCRAMBLER (FUNCTIONAL DIAGRAM)



NOTE 1: For STS-Nc SPEs, the STS Path Overhead is only allocated for the first STS-1.
NOTE 2: Only defined for STS-1 #1 of OC-N line signal.

FIGURE 43 - AN EXAMPLE OF STS-1 FRAME & OC-N LINE SIGNAL COMPOSITION

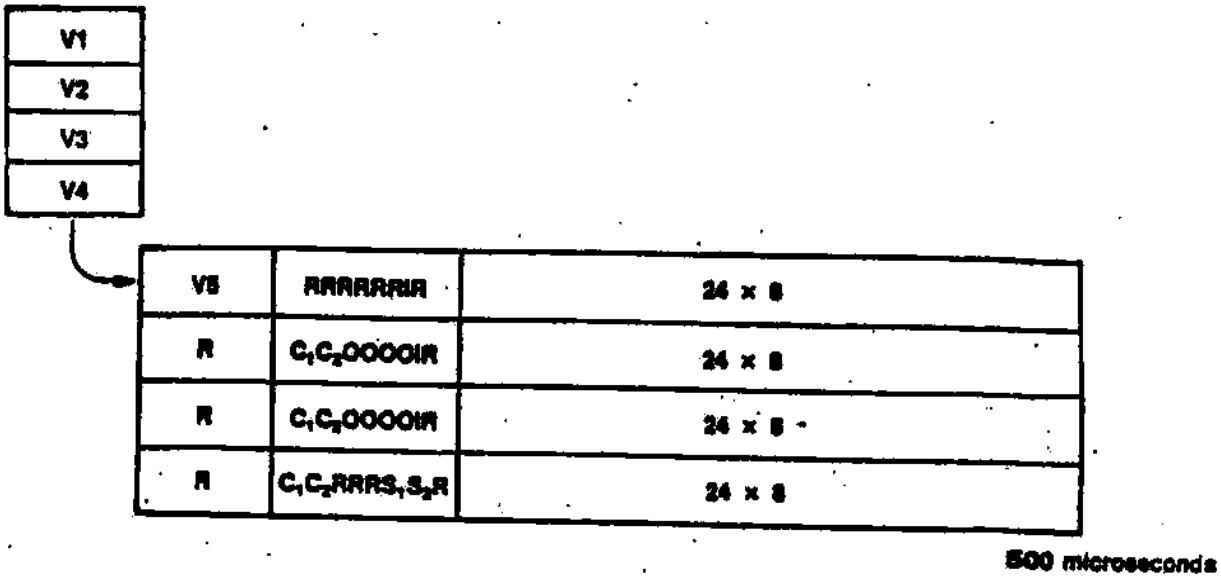


FIGURE 44 – ASYNCHRONOUS MAPPING FOR DS1 PAYLOAD

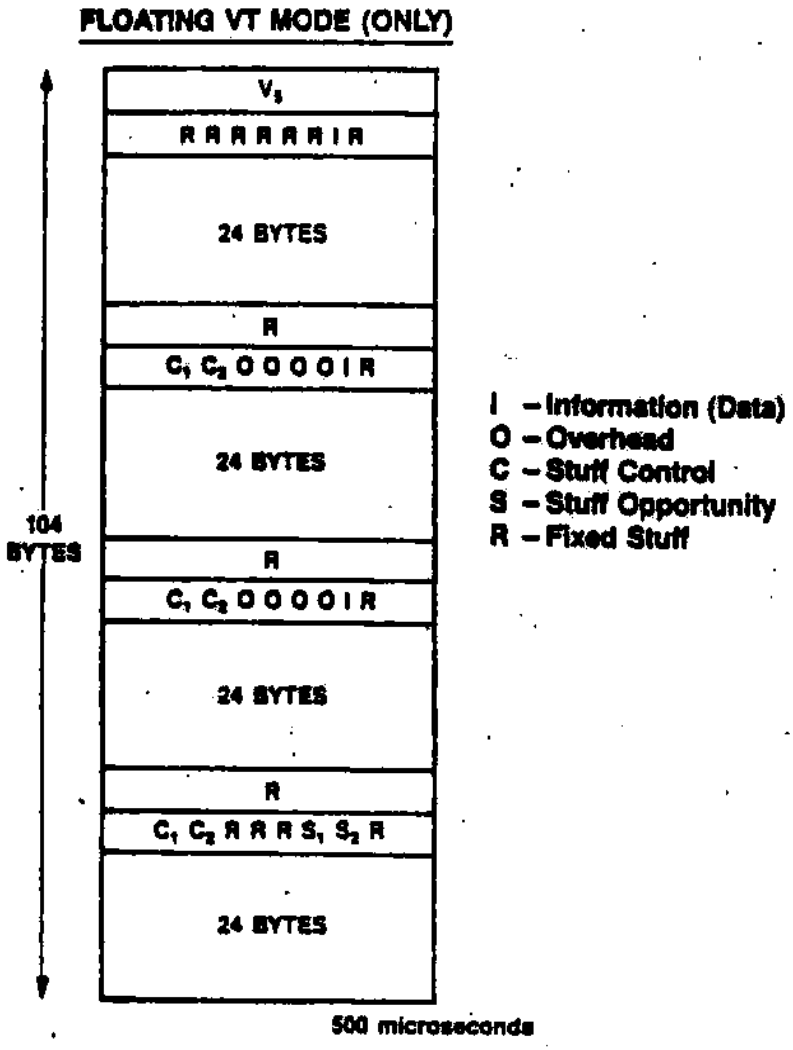


FIGURE 45 – ASYNCHRONOUS MAPPING FOR DS1 PAYLOAD

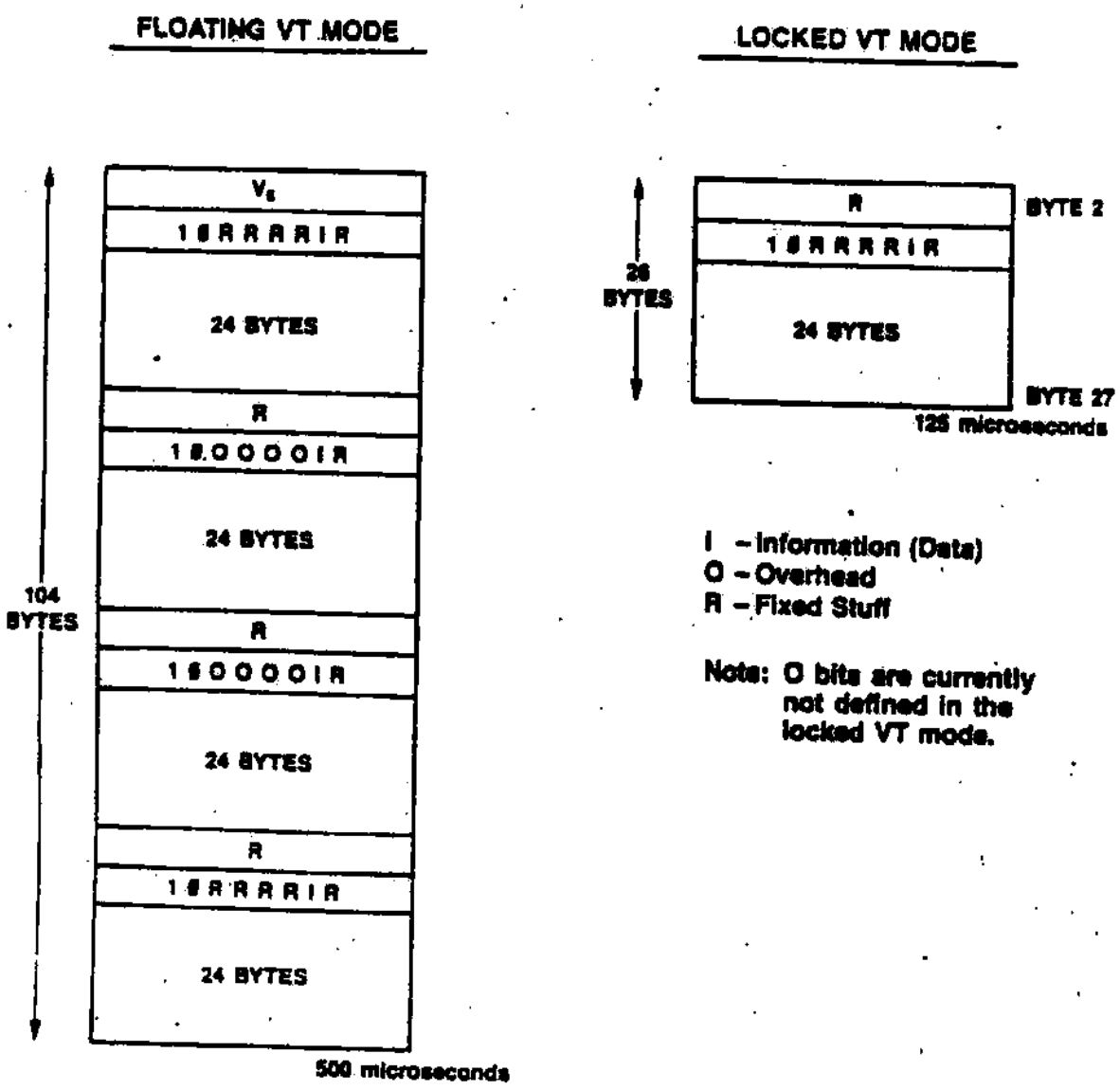
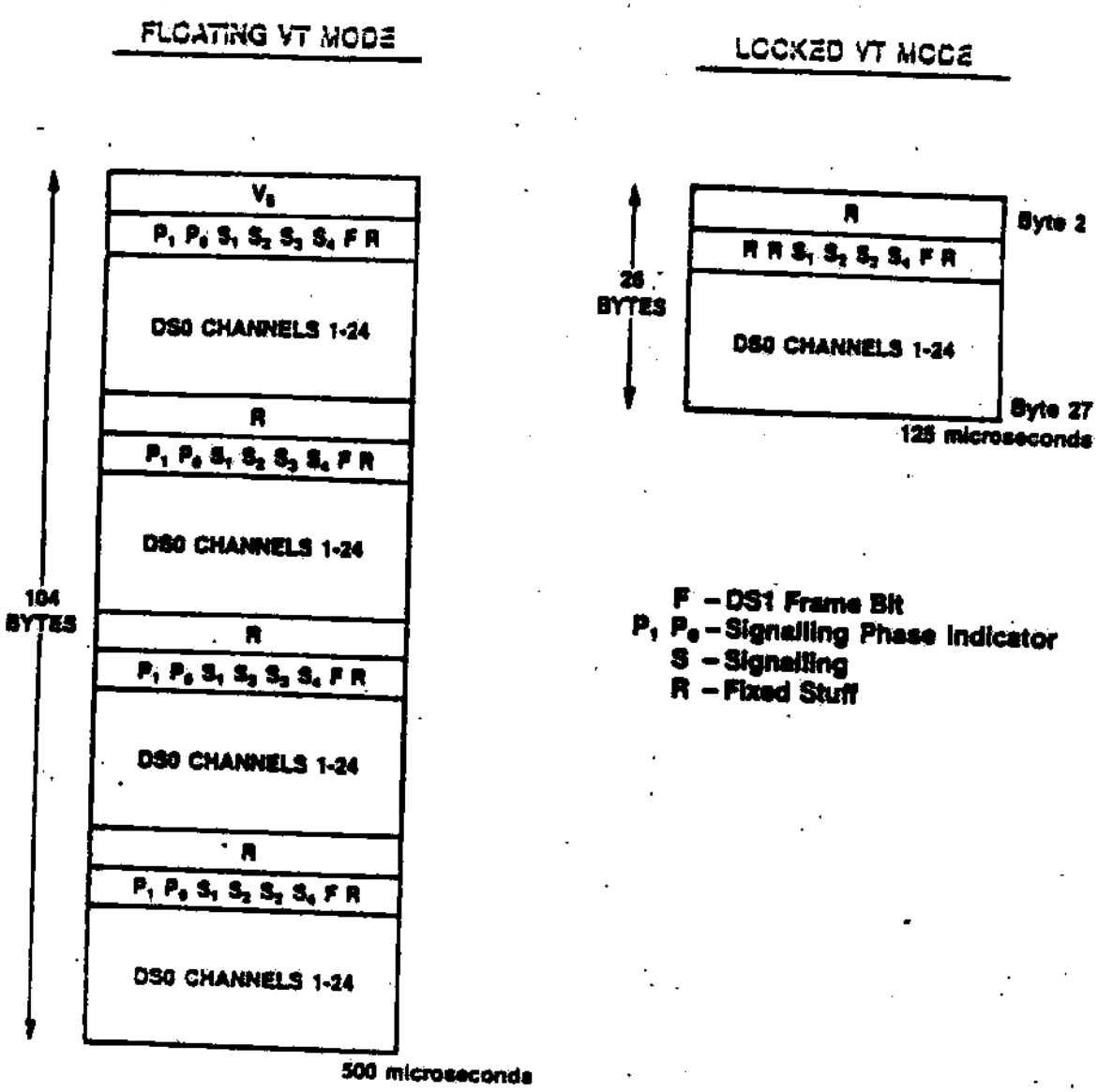


FIGURE 46 – BIT SYNCHRONOUS MAPPING FOR DS1 PAYLOAD



P_1P_2 = 00 on the first signaling byte of the superframe.

FIGURE 47 – BYTE SYNCHRONOUS MAPPING FOR DS1 PAYLOAD

LOCKED

FLOATING

SIGNALING

H4 VALUE					2 STATE				4 STATE				16 STATE				
P_1	P_2	SI_2	SI_1	T	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	S_1	S_2	S_3	S_4	P_1P_2
0	0	0	0	0	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	00
0	0	0	0	1	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	00
0	0	0	1	0	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	00
0	0	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	00
0	0	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	00
0	0	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	00
0	1	0	0	0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	B_1	B_2	B_3	B_4	01
0	1	0	0	1	A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	B_5	B_6	B_7	B_8	01
0	1	0	1	0	A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	B_9	B_{10}	B_{11}	B_{12}	01
0	1	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	B_{13}	B_{14}	B_{15}	B_{16}	01
0	1	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	B_{17}	B_{18}	B_{19}	B_{20}	01
0	1	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	B_{21}	B_{22}	B_{23}	B_{24}	01
1	0	0	0	0	A_1	A_2	A_3	A_4	A_1	A_2	A_3	A_4	C_1	C_2	C_3	C_4	10
1	0	0	0	1	A_5	A_6	A_7	A_8	A_5	A_6	A_7	A_8	C_5	C_6	C_7	C_8	10
1	0	0	1	0	A_9	A_{10}	A_{11}	A_{12}	A_9	A_{10}	A_{11}	A_{12}	C_9	C_{10}	C_{11}	C_{12}	10
1	0	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	A_{13}	A_{14}	A_{15}	A_{16}	C_{13}	C_{14}	C_{15}	C_{16}	10
1	0	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	A_{17}	A_{18}	A_{19}	A_{20}	C_{17}	C_{18}	C_{19}	C_{20}	10
1	0	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	A_{21}	A_{22}	A_{23}	A_{24}	C_{21}	C_{22}	C_{23}	C_{24}	10
1	1	0	0	0	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	D_1	D_2	D_3	D_4	11
1	1	0	0	1	A_5	A_6	A_7	A_8	B_5	B_6	B_7	B_8	D_5	D_6	D_7	D_8	11
1	1	0	1	0	A_9	A_{10}	A_{11}	A_{12}	B_9	B_{10}	B_{11}	B_{12}	D_9	D_{10}	D_{11}	D_{12}	11
1	1	0	1	1	A_{13}	A_{14}	A_{15}	A_{16}	B_{13}	B_{14}	B_{15}	B_{16}	D_{13}	D_{14}	D_{15}	D_{16}	11
1	1	1	0	0	A_{17}	A_{18}	A_{19}	A_{20}	B_{17}	B_{18}	B_{19}	B_{20}	D_{17}	D_{18}	D_{19}	D_{20}	11
1	1	1	0	1	A_{21}	A_{22}	A_{23}	A_{24}	B_{21}	B_{22}	B_{23}	B_{24}	D_{21}	D_{22}	D_{23}	D_{24}	11

FIGURE 48 - OUT SLOT SIGNALING ASSIGNMENTS
24 CH. SIGNALING OPERATIONS

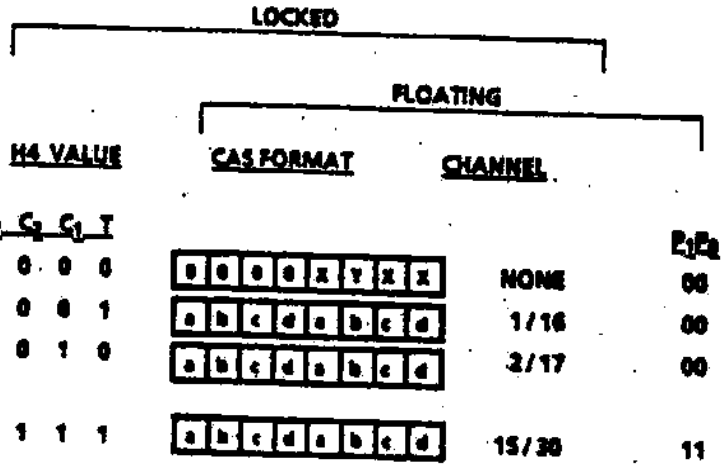


FIGURE 49 - OUT SLOT SIGNALING ASSIGNMENTS 30 CH. SIGNALING OPERATIONS

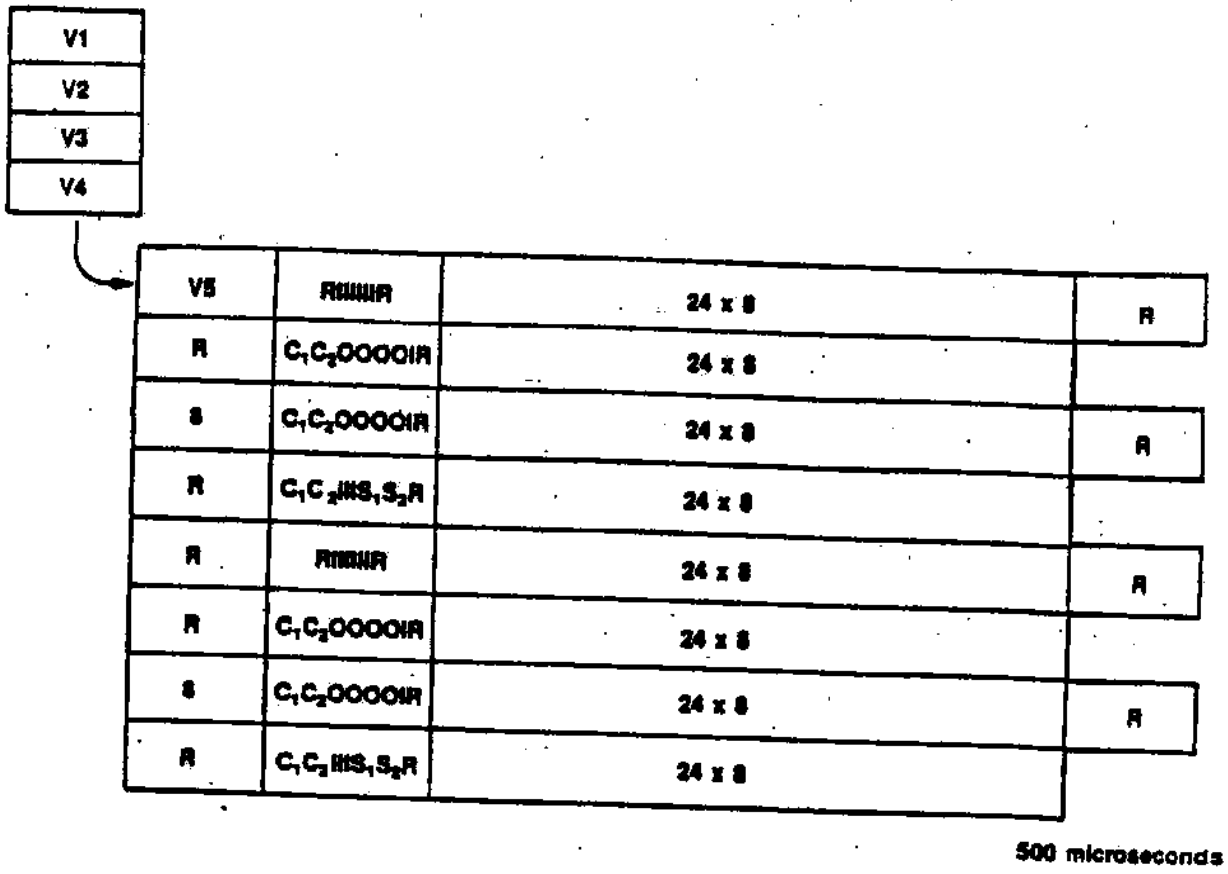


FIGURE 50 – ASYNCHRONOUS MAPPING FOR DS1C PAYLOAD

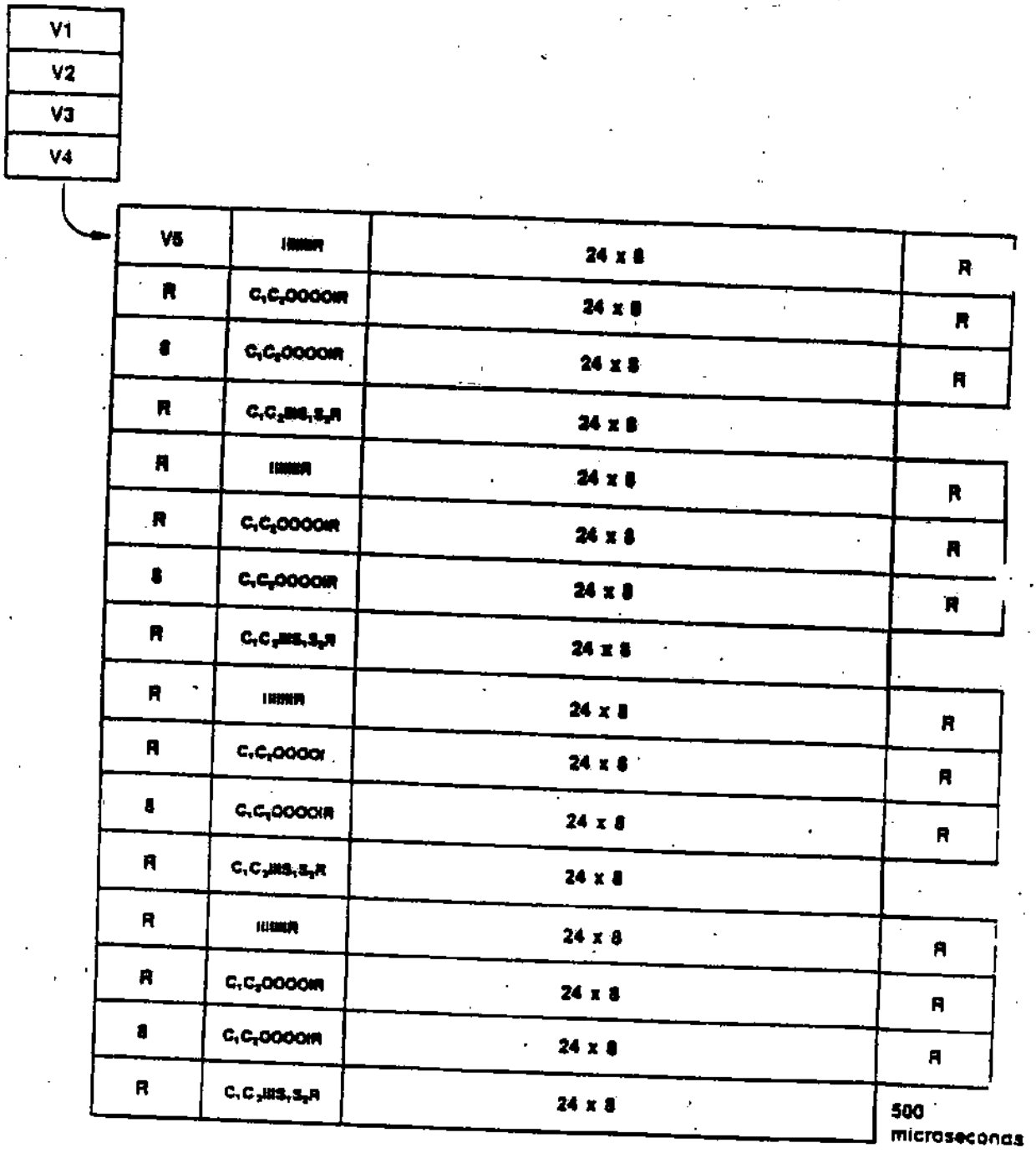


FIGURE 51 – ASYNCHRONOUS MAPPING FOR DS2 PAYLOAD

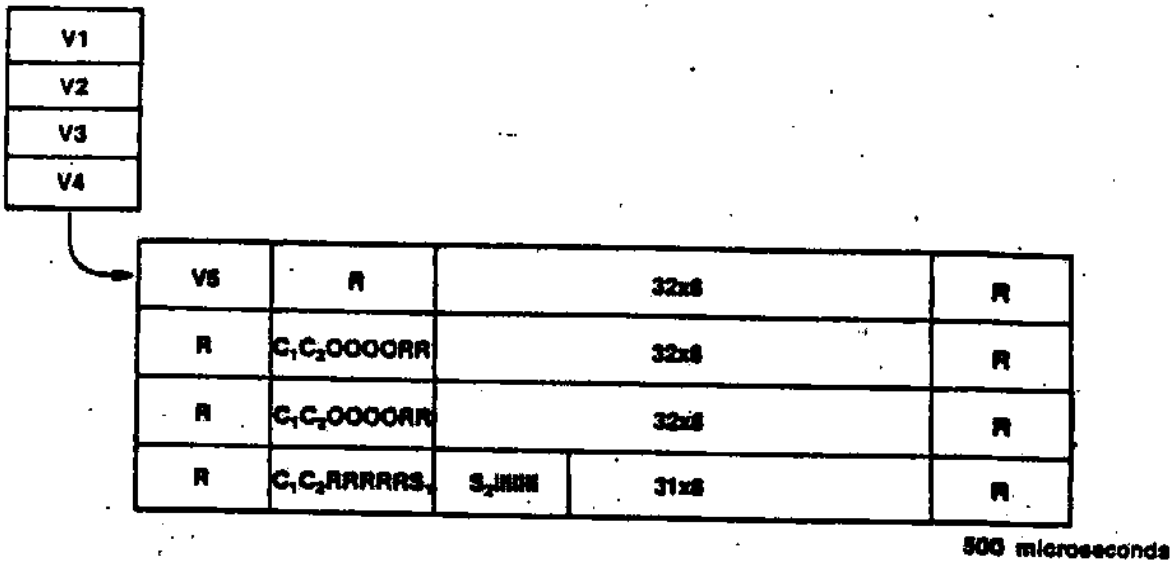


FIGURE 52 – ASYNCHRONOUS MAPPING FOR 2.048 Mbit/s PAYLOAD

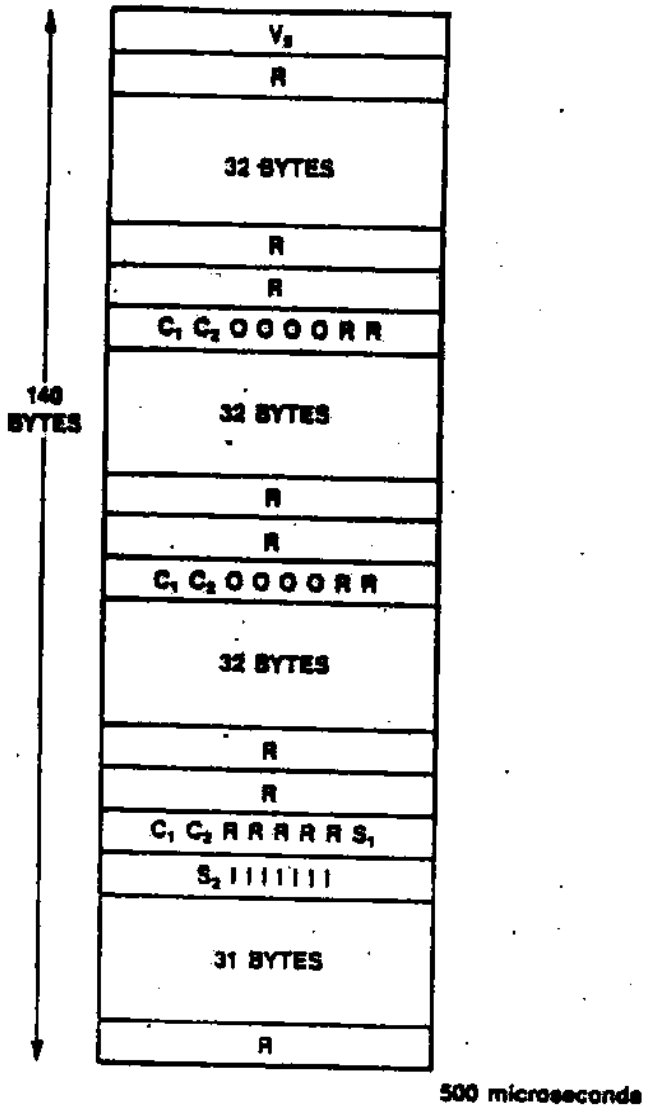


FIGURE 53 – ASYNCHRONOUS MAPPING FOR 2.048 Mbit/s PAYLOAD

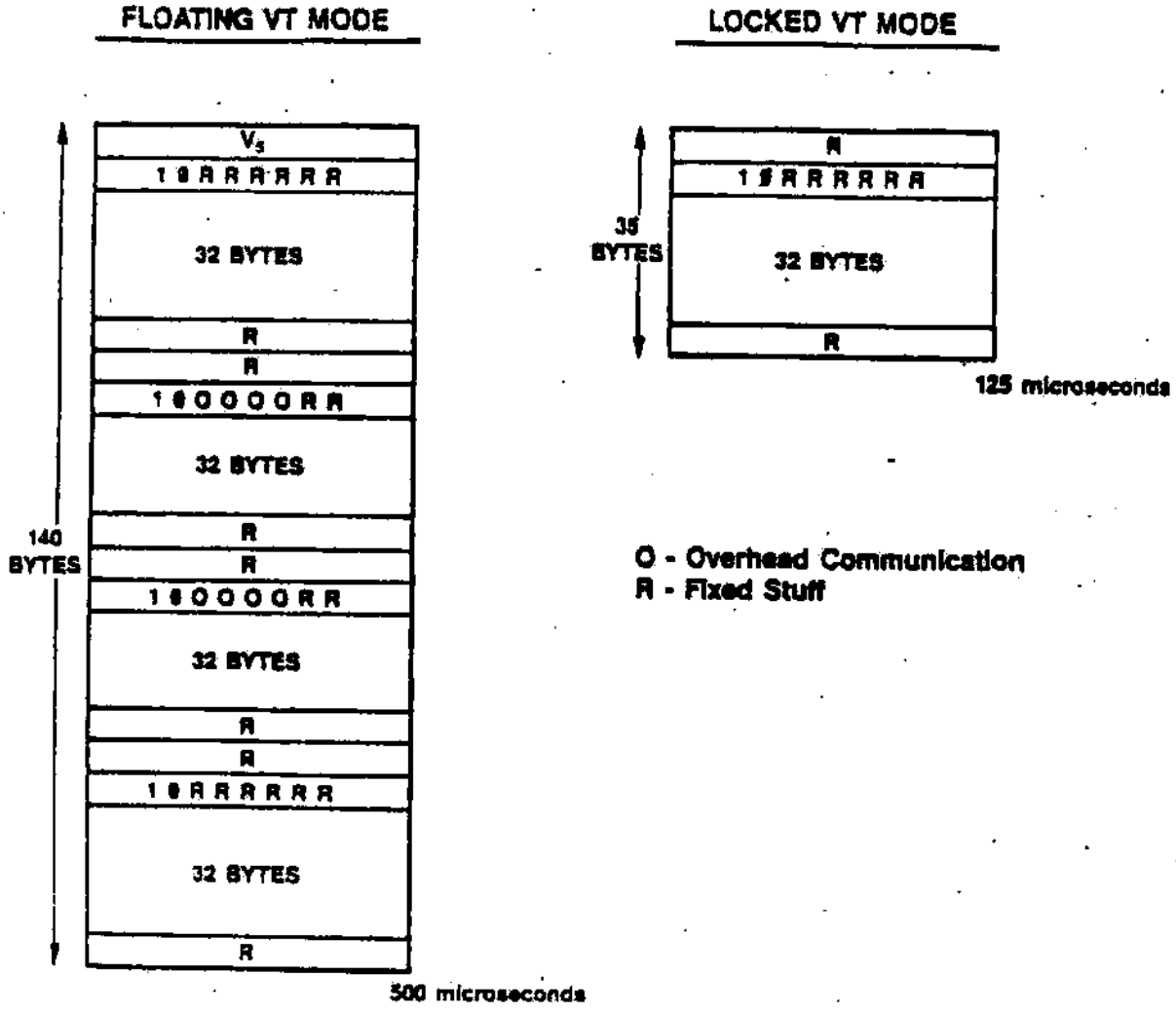
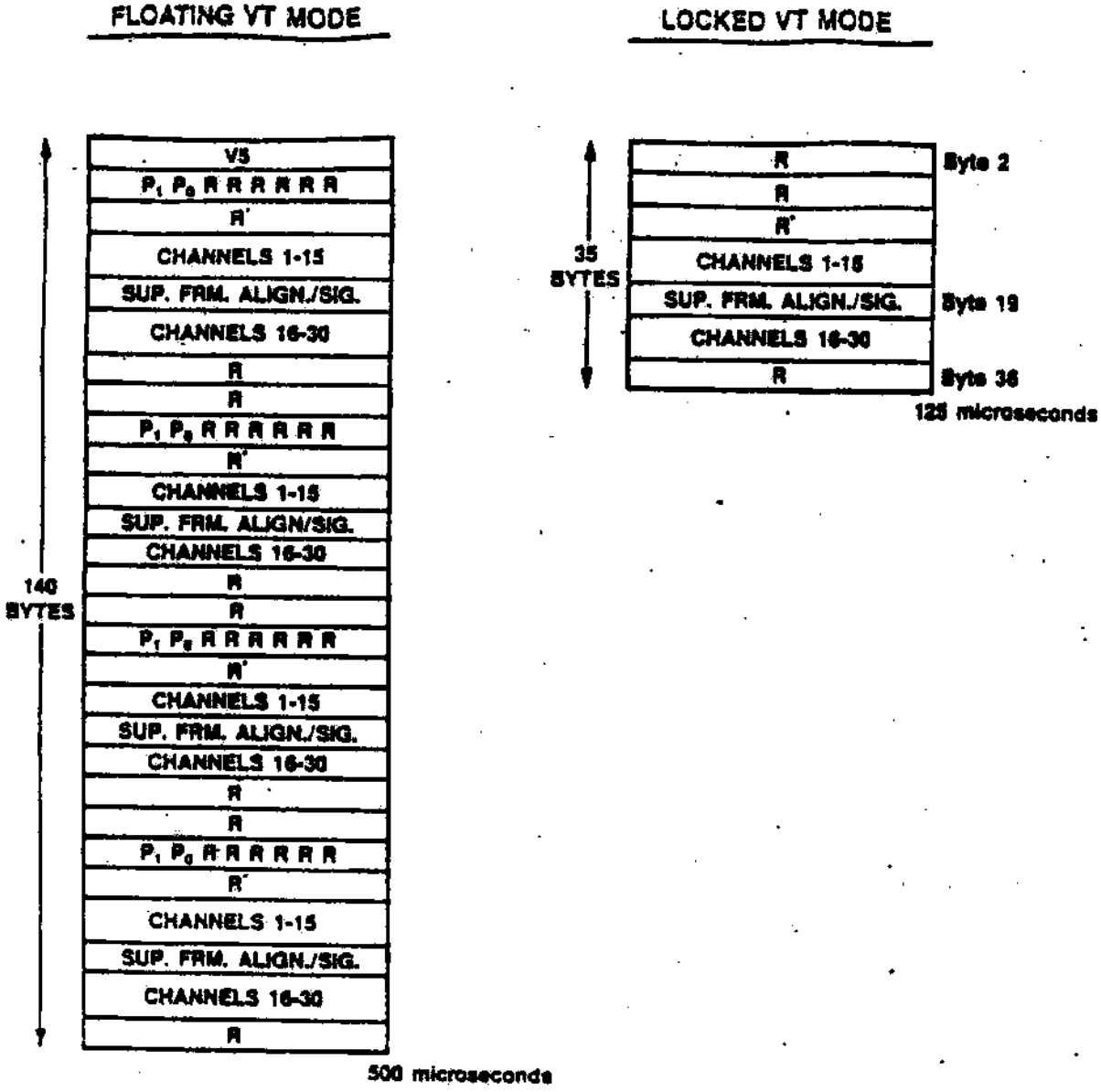


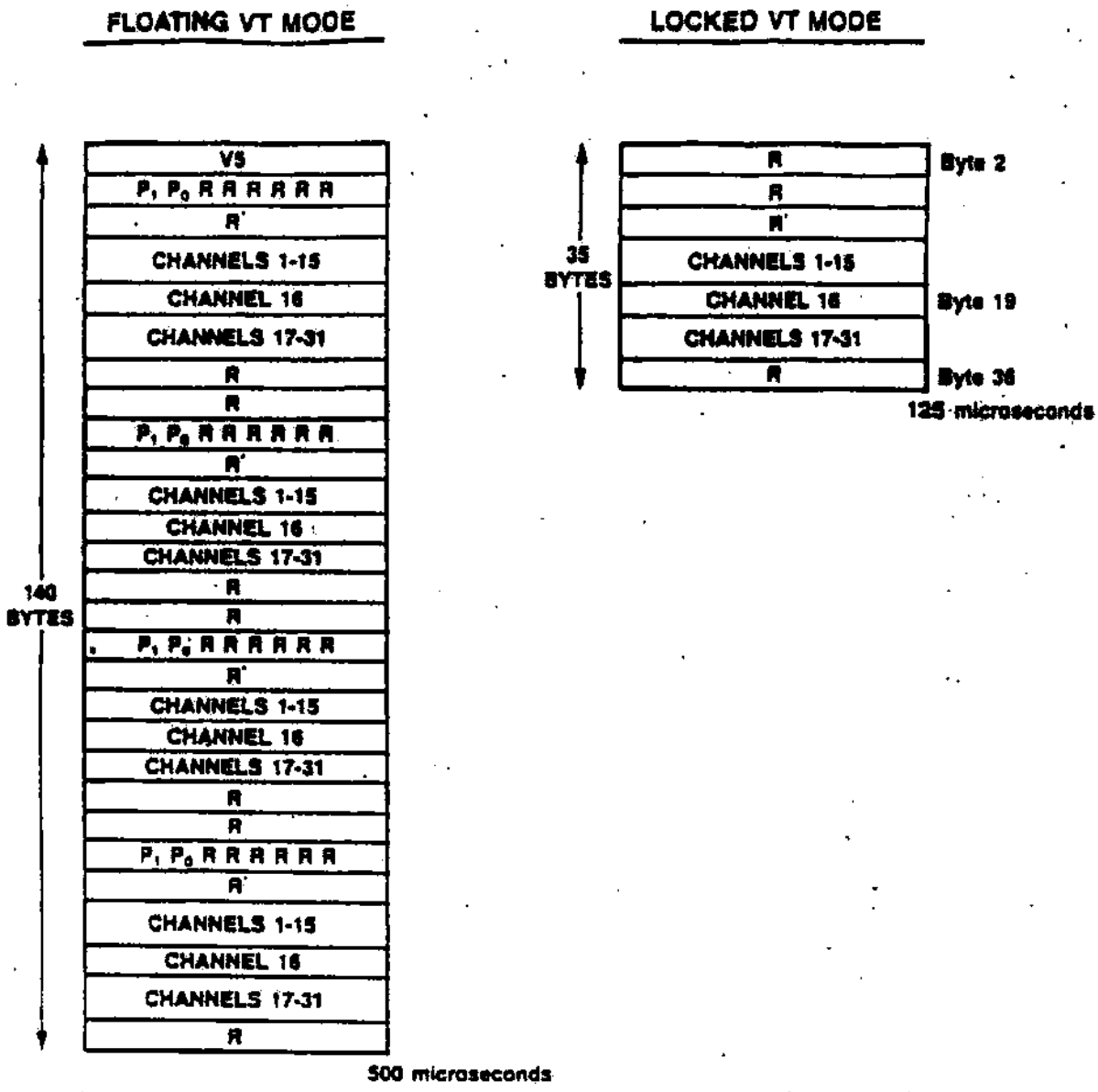
FIGURE 54 – BIT SYNCHRONOUS MAPPING FOR 2.048 Mbit/s PAYLOAD



*MAY BE USED FOR TIMESLOT 0 IF REQUIRED

P_1 P_0 = 00 AT THE START OF THE SIGNALING FRAME
ON THE FIRST BYTE OF THE SIGNALING FRAME

FIGURE 55 – BYTE SYNCHRONOUS MAPPING FOR 2.048 Mbit/s PAYLOAD 30 CHANNEL WITH CAS



*MAY BE USED FOR TIMESLOT 0 IF REQUIRED

P_1 P_0 = 00 AT THE START OF THE SIGNALING FRAME
ON THE FIRST BYTE OF THE SIGNALING FRAME

FIGURE 56 – BYTE SYNCHRONOUS MAPPING FOR 2.048 Mbit/s PAYLOAD
31 CHANNEL WITH CCS

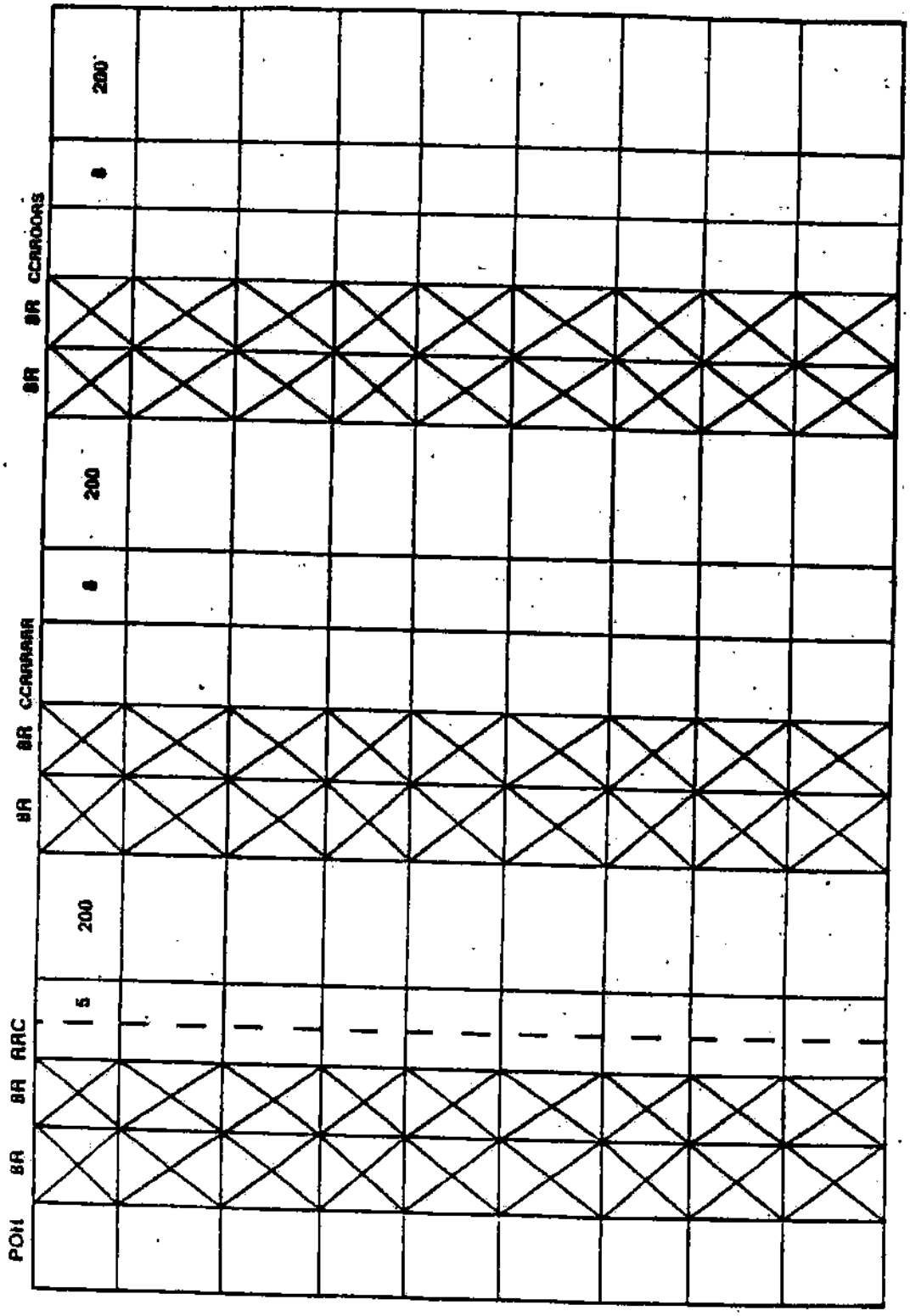


FIGURE 57 – ASYNCHRONOUS MAPPING FOR DS3 PAYLOAD

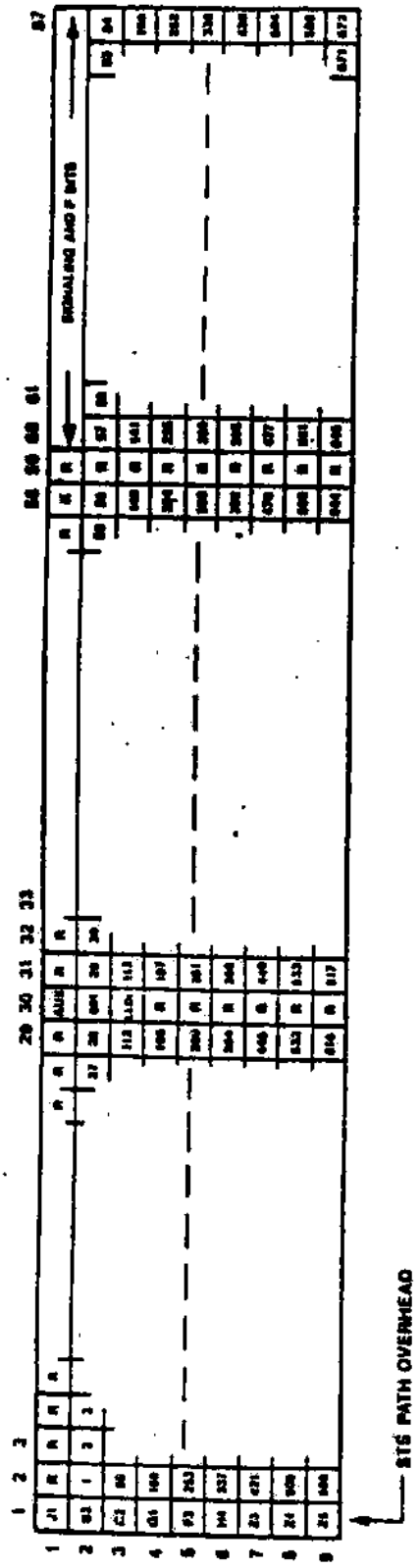
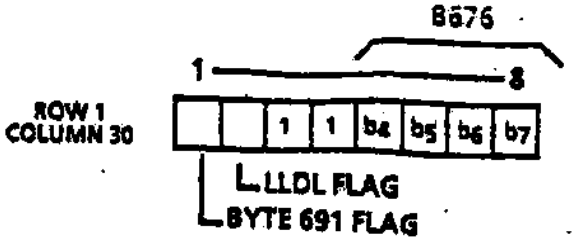
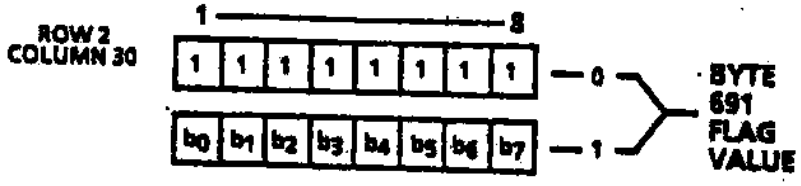


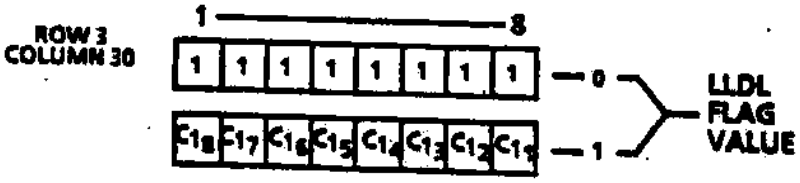
FIGURE 58 – BYTE OBSERVABLE SYNTRAN MAPPING



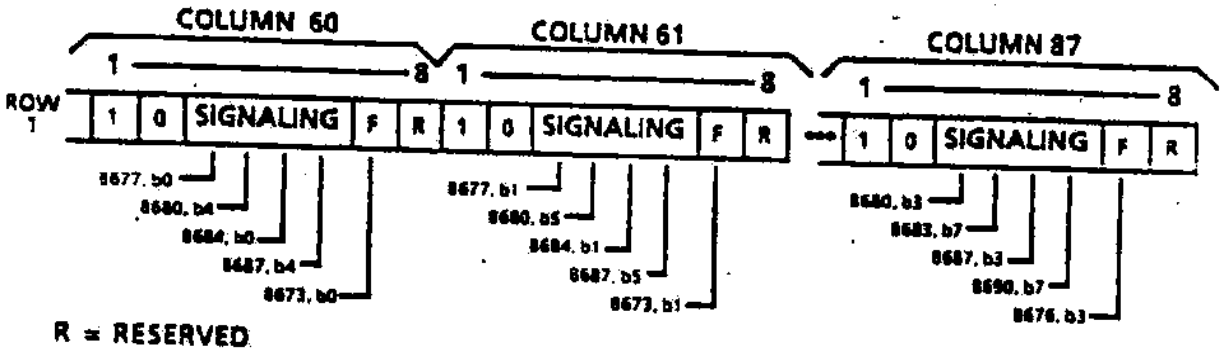
A - AUXILIARY BYTE



8 - BYTE 691



C - LOW LEVEL DATA LINK



D - F & SIGNALING BITS

FIGURE 59- ADDITIONAL SYNTRAN INFORMATION MAPPING

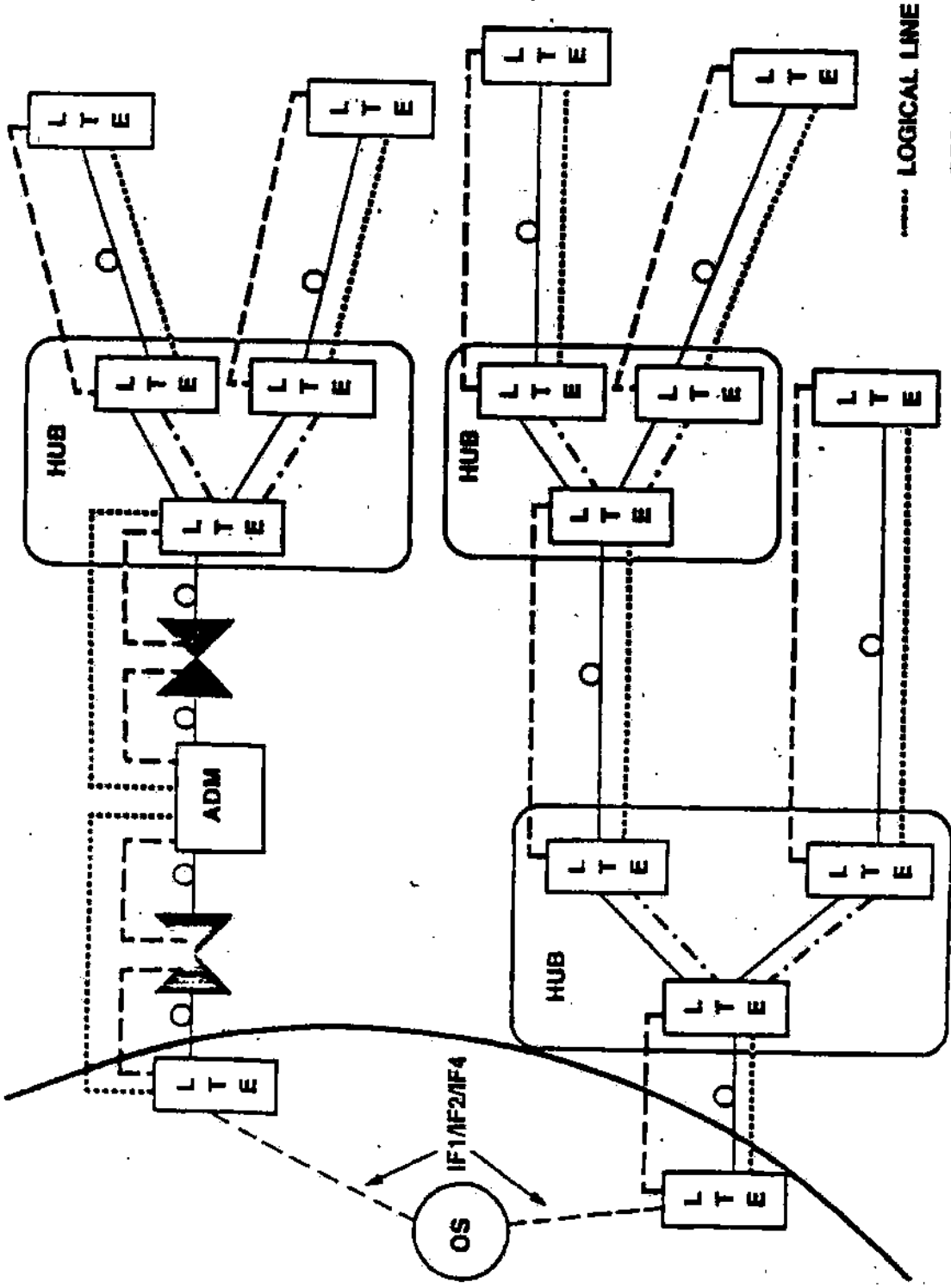


FIGURE 6D – DATA COMMUNICATIONS CHANNEL USAGE

Appendix A. Timing and Synchronization Application Guidelines

(This Appendix is not part of American National Standard [ ], but is included for information only.)

Integrating synchronous optical equipment into the existing telecommunications network requires appropriate synchronization engineering. Section A1 provides recommendations for synchronizing synchronous optical equipment. Section A2 provides timing recommendations describing synchronous optical equipment configurations which (1) provide timing to the Building Integrated Timing Supply (BITS), (2) receive timing from the BITS, and (3) utilize loop timing. Section A3 provides synchronous optical network clock performance recommendations addressing (1) transients on the input timing signal and (2) short term stability.

A1. Clock Application Guidelines

Figure A1, parts (A) - (E) provides illustrative examples of clock applications for synchronous optical terminals, add/drop multiplexers (ADMs), concentrators (hubs), digital cross-connect systems (DCSs), and through repeaters (regenerators). The following subsections describe these clock applications.

In terminal, ADM, concentrator and DCS applications, synchronous optical equipment needs to be integrated into the existing synchronization timing architecture. This architecture is based on the use of a hubbing concept for timing distribution and is embodied by the BITS concept described in Reference A1 (see Section A4). The following paragraph summarizes the BITS concept.

Figure A2 illustrates an example of the BITS architecture. The hubbing concept for timing distribution allows for one clock in a building (denoted the BITS) to control the timing of all clocks within the building. The clock selected as the BITS is of the highest stratum level within the building and receives external reference traceable to a Primary Reference Source (PRS).

In the Central Office (CO), the BITS concept should be used to provide reference timing to synchronous optical equipment as described in Section A2.1. In addition, to allow for evolution to synchronous optical network based timing distribution, the synchronous optical equipment in these applications should provide the capability to time the BITS as described in Section A2.2.

Synchronous optical terminal equipment in small end link central offices, loop plant or customer location may utilize loop timing without violating the stratum 3 clock requirements.

A2. Timing Recommendations

A2.1 Receiving Timing Reference from Office BITS Clock

As a minimum requirement, synchronous optical equipment should accept two DS1 timing signals as defined in Reference A2 (see Section A4). The future use of an STS-1 rate timing signal requires further study.

A2.2 Providing a Synchronous Optical Network based Timing Reference to the Office BITS Clock

Synchronous optical equipment should have the capability to supply timing reference to the BITS clock derived from an incoming OC-N signal. A framed, all ones DS1 timing signal should be supplied. A DS1 AIS signal should be inserted whenever the OC-N signal is not suitable as a timing reference. The future use of an STS-N rate timing signal to supply the office BITS requires further study.

A2.3 Receiving Timing Reference from the Incoming OC-N Signal (Loop Timing)

Synchronous optical equipment configured for this mode of operation should have the capability to directly derive clock timing from the incoming OC-N signal. All transmitted OC-N signal(s) are timed from this clock. When the OC-N signal is not able to provide reference timing, the equipment clock should continue to operate to generate proper maintenance signals.

A3. Clock Timing Performance

A3.1 Phase Transients

Clocks utilized in synchronous optical equipment should be designed so that transient timing impairments (e.g., error bursts, phase hits, short outages) on incoming references do not produce errors on outgoing signals.

Switching of duplex clock elements should not result in errors on outgoing signals. Therefore, the amount of phase discontinuity caused by clock protection switching must be constrained. In addition, all outgoing DS1 signals should meet the requirements specified in Reference A2.

A3.2 Clock Short Term Stability

In order to constrain the probability of bursty pointer adjustments and avoid spill in the desynchronizer buffer, the standard addresses the short term stability of clocks utilized to provide timing to synchronous optical equipment. The short term stability of clocks utilized to provide timing to synchronous optical equipment shall provisionally meet the mask given in Figure 4 of the standard. The final requirement will be no more restrictive than this provisional requirement.

The mask allows a maximum rms phase variation of 150 ns for observation times greater than 100 seconds; this reflects a clock transfer function with maximum bandwidth of 0.01 Hz. Compliance with this mask may be tested by providing an input reference with bandlimited white noise jitter of 1 microsecond p-p. The jitter should be bandlimited with a 3 dB cutoff of 150 Hz.

A4. References

A1. TA-NPL-000436, Digital Network Synchronization Plan, Issue 1, November, 1986

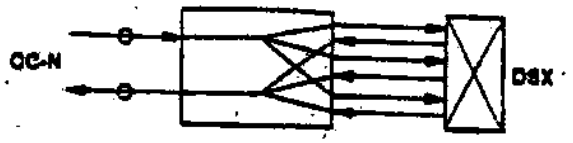
A2. TA-TSY-000378, Timing Signal Generator, Issue 1, April, 1986

Copies of these documents may be obtained from:

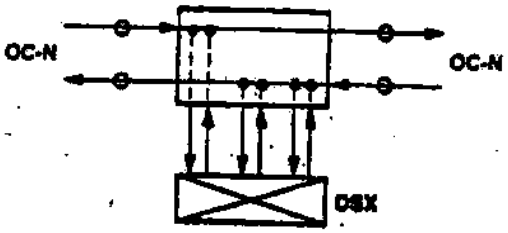
Information Exchange Manager
Bellcore
435 South St., Room 2T-147
Morristown, NJ 07960-1961

T1 551700

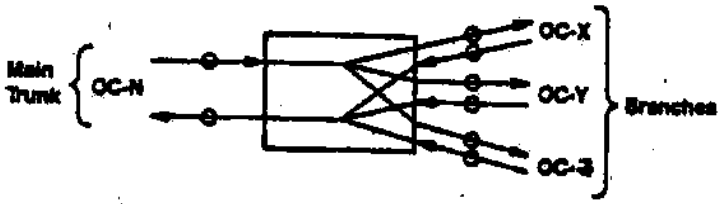
A. Terminal



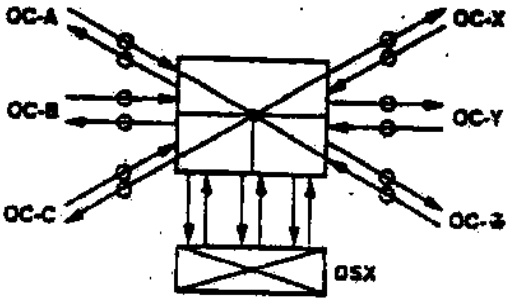
B. ADM



C. Concentrator (Hub)



D. DCS



E. Thru-Repeater (Regenerator)

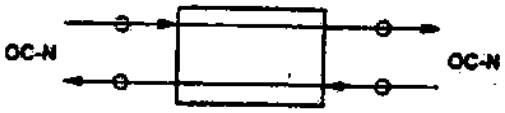


FIGURE A1 – ILLUSTRATION OF CLOCK APPLICATIONS WITH SYNCHRONOUS OPTICAL EQUIPMENT

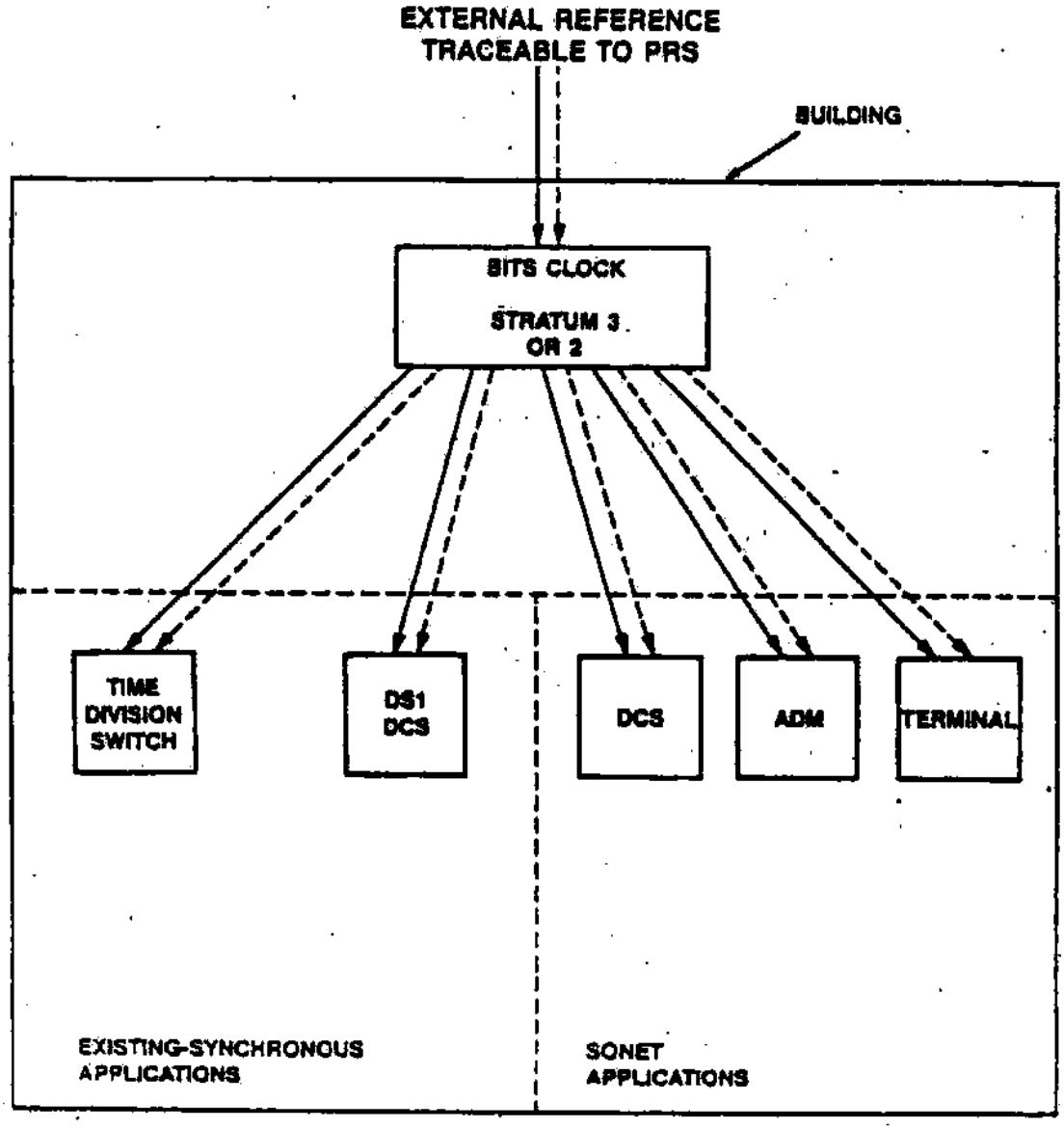


FIGURE A2 – EXAMPLE OF BITS "HUBBING" ARCHITECTURE

T1 551700

Appendix B. 1:n Bi-Directional Switching Example

(This Appendix is not part of American National Standard [ ], but is included for information only.)

Figure B1 and Table B1 illustrate the protection switching action for a 1:n bi-directional switching example.

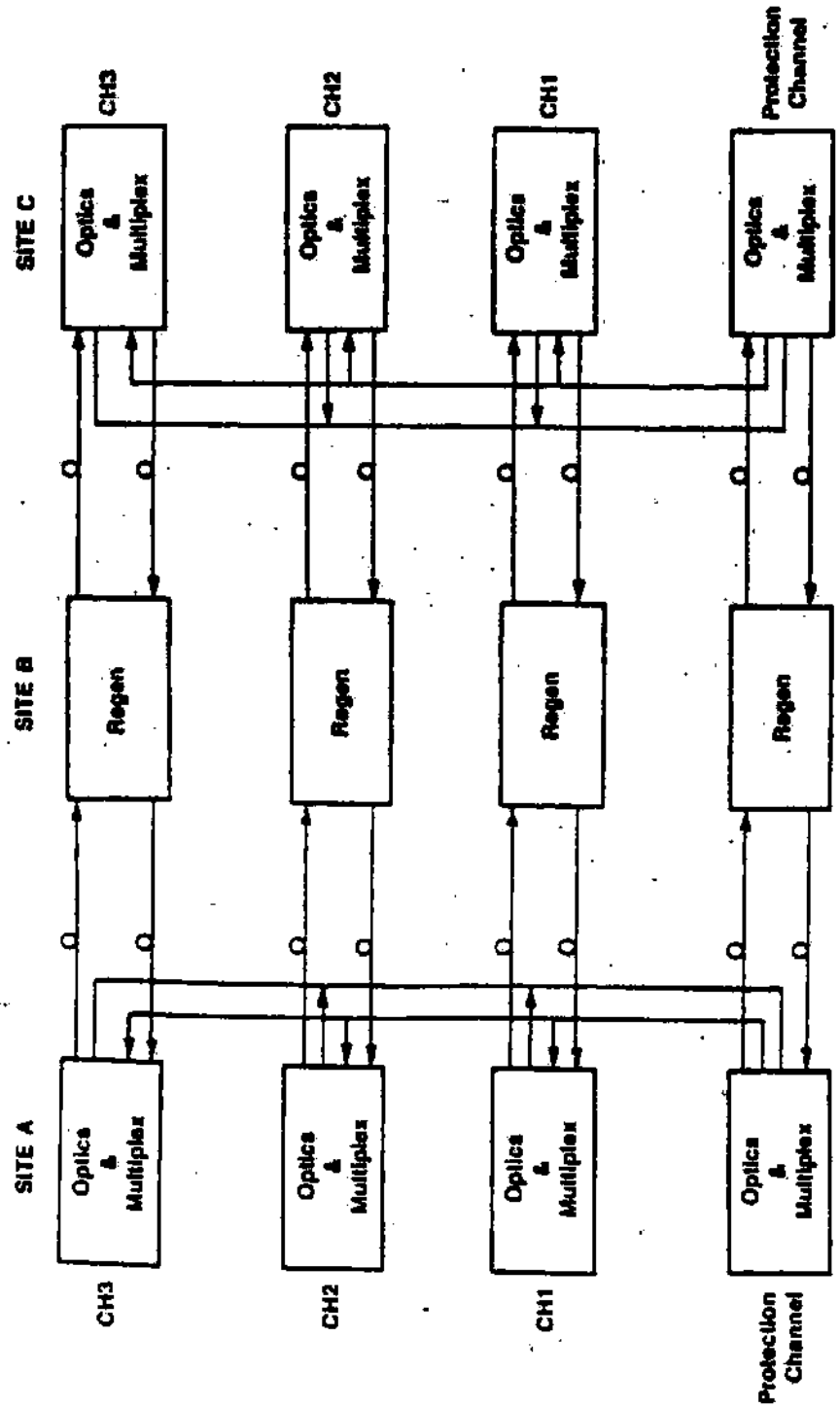


FIGURE B1 – 1:n PROTECTION SWITCHING EXAMPLE

FAULT/SWITCH CONDITIONS	APS BYTES				ACTION	
	C → A		A → C		AT C	AT A
	BYTE K1	BYTE K2	BYTE K1	BYTE K2		
NO FAULTS (PROTECTION CHANNEL IS NOT IN USE BRIDGED TO CHAN 3 TO PROVIDE A VALID SIGNAL.)	00000000	00111000	00000000	00111000		
CHAN 2 DEGRADE DIRECTION A ▶ C	10100010	00111000	00000000	00111000	DETECTS FAULT ORDER BRIDGE CHAN 2	
	10100010	00111000	01100010	00111000	-	BRIDGE CHAN 2 ORDER BRIDGE CHAN 2
	10100010	00101000	00100010	00101000	COMPLETE SWITCH CHAN 2 BRIDGE CHAN 2	-
	10100010	00101000	00100010	00101000	-	COMPLETES BIDIRECTIONAL SWITCH CHAN 2
CHAN 1 FAIL DIRECTION C ▶ A (THIS PREMPTS THE CHAN 2 SWITCH)	10100010	00101000	11000001	00101000	DETECTS FAULT REQUEST BRIDGE CHAN 1 DROPS CHANNEL 2 SWITCH	-
	01100001	00111000	11000001	00101000	BRIDGE CHAN 1 ORDER CHAN 1 BRIDGE DROP CHAN 2 SWITCH	-
	01100001	00111000	11000001	00111000	-	COMPLETES CHAN 1 SWITCH BRIDGES CHAN 1
	01100001	00111000	11000001	00111000	COMPLETES BIDIRECTIONAL SWITCH CHAN 1	-

TABLE B1 – 1:n BIDIRECTIONAL SWITCHING EXAMPLE

FAULT/SWITCH CONDITION	APS BYTES				ACTION	
	C → A		A → C			
	BYTE K1	BYTE K2	BYTE K1	BYTE K2	AT C	AT A
CHAN 1 REPAIRED (CHAN 2 STILL DEG SO CHAN 2 WILL NOW SWITCH)	00100001	00011000	01100001	00011000	-	GO TO WAIT TO RESTORE CHAN 2
	10100010	00011000	01100001	00011000	ORDER BRIDGE CHAN 2 DROP CHANNEL 1 SWITCH	-
	10100010	00011000	00100010	00011000	-	BRIDGE CHAN 2 ORDER BRIDGE CHAN 2 DROP CHAN 1 SWITCH
	10100010	00101000	00100010	00101000	SWITCH CHAN 2 BRIDGE CHAN 2	-
	10100010	00101000	00100010	00101000	-	COMPLETE BIDIRECTIONAL SWITCH CHAN 2
CHAN 2 REPAIRED	01100010	00101000	00100010	00101000	GO TO WAIT TO RESTORE CHAN 2	-
WAIT TO RESTORE EXPIRES	00000000	00101000	00100010	00101000	DROP SWITCH ON CHAN 2 DROP BRIDGE ORDER CHAN 2	-
	00000000	00101000	00000000	00111000	-	DROP BRIDGE ON CHAN 2 DROP SWITCH ON CHAN 2 DROP BRIDGE ORDER CHAN 2
NO FAULTS PROTECTION CHANNEL IS NOT IN USE BRIDGED TO CHAN 3 TO PROVIDE A VALID SIGNAL	00000000	00111000	00000000	00111000	DROP BRIDGE ON CHAN 2	-

TABLE B1 – 1:n BIDIRECTIONAL SWITCHING EXAMPLE (CONTINUED)

Case 1:04-cv-00876-GMS Document 121-2 Filed 03/24/2006 Page 117 of 117